

LCFC Confidential

S750-ACH MB Schematics Document

S750 Renoir/Cezanne with DDR4

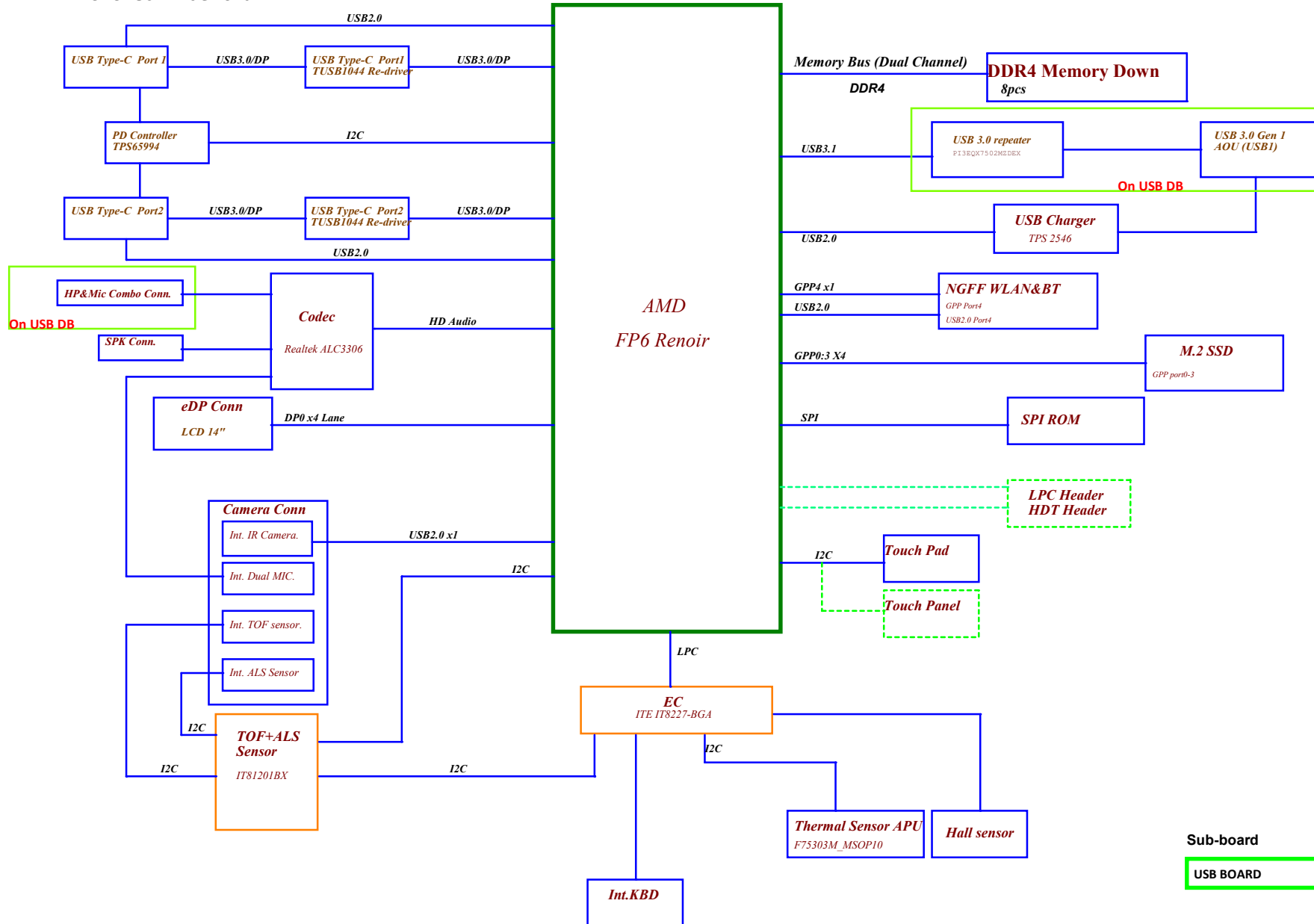
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REV: 0.3

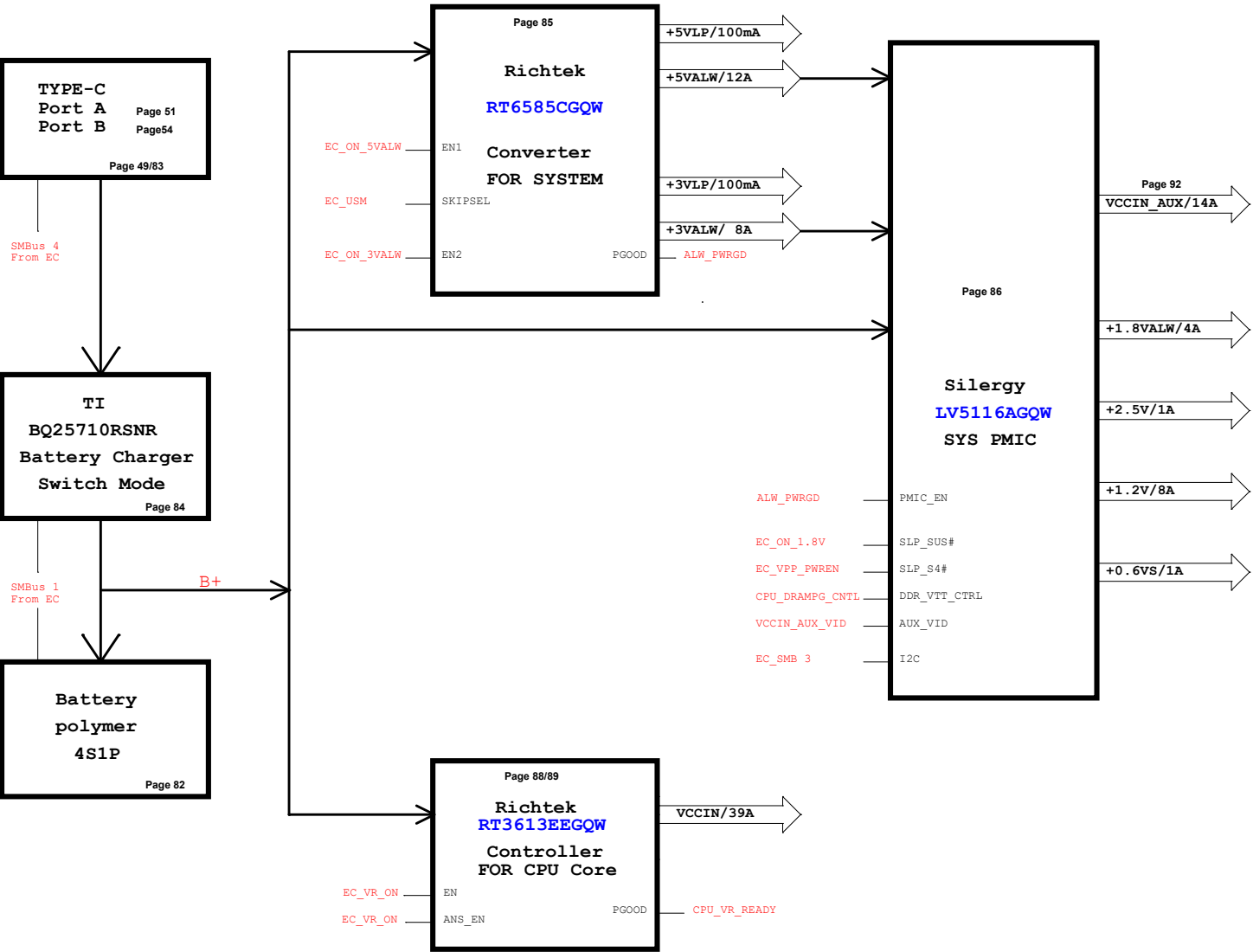
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S750 Renoir/Cezanne Schematic Block Diagram

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Block Diagram_Power



Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane \ State	B+ +3VL +5VL	+3VALW +5VALW	+0.75VALW +1.8VALW +3VALW_CPU	+0.6VS +1.2V +2.5V_DDR	+5VS +3VS	+VCCSTG
S0	O	O	O	O	O	O
S0Ix	O	O	O	O	O	X ***
S3	O	O	O	O	X	X
S3 Battery only	O	O	O	O	X	X
S5 S4 AC Only	O	O	X ***	X	X	X
S5 S4 Battery only	O	O	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X	X

HSIO Matrix

HSIO PORT	Function
USB2.0	0 Type C Port 1
	1 Type A AOU
	2 Camera
	3 NC
	4 TYPE C Port 2
	5 NC
	6 NC
	7 BT
USB3.0	0 Type C Port 1
	1 USB A AOU
	4 Type C Port 2
	5 NC
GPP PCIE	0 NC
	1 NC
	2 NC
	3 NC
	4 NC
	5 NC
	6 NC
	7 NC
	8 SSD
	9 SSD
	10 SSD
	11 SSD

SMBUS Control Table

Source \ Slave	EC IT8227C				PCH			PD TPS65994
	EC_SMB_0 +3VS	EC_SMB_1 +3VL_EC	EC_SMB_3 +3VL_EC	EC_SMB_4 +3VL_EC	PCH_I2C_0 +1.8VS	PCH_I2C_1 +3VALW_PCH	ISH_I2C_0 +3VS	PD_I2C_3 VCC3_LDO_PD
DGPU								
Memory Down	X	X	X	X	X	X	X	X
PD FW Update					V +1.8VS			
BATT	X	V +3VL_EC	X	X	X	X	X	X
Charger	X	V +3VL_EC	X	X	X	X	X	X
WLAN	X	X	X	X	X	X	X	X
PMIC	X	X	X	X	X	X	X	X
IMVP9	X	X	X	X	X	X	X	X
Thermal Sensor	V +3VS	X	X	X	X	X	X	X
Sensorhub			V +3VL_EC					
TP	X	X	X	X	X	V +3VS	V +3VALW_PCH	X
Light Sensor	X	X	X	X	X	X	V +3VALW_PCH	X
Re-Timer	X	X	X	X	X	X	X	V VCC3_LDO_PD
PD	X	X	X	V +3VL_EC	X	X	X	X

EC SMBus0 address

Device	Address
DGPU	
Thermal Sensor(NCT7718W)	
Thermal Sensor(NCT7719W)	1001_101xb
TOF	

PCH SML0 address

Device	Address
Re-Timer	TBD

PD I2C3 address

Device	Address
Re-Timer	TBD

EC SMBus1 address

Device	Address
Smart Battery	0x16
Charger	0x12

PCH SML1 address

Device	Address
PD	TBD

EC SMBus3 address

Device	Address
IMVP9	
PMIC	0x34

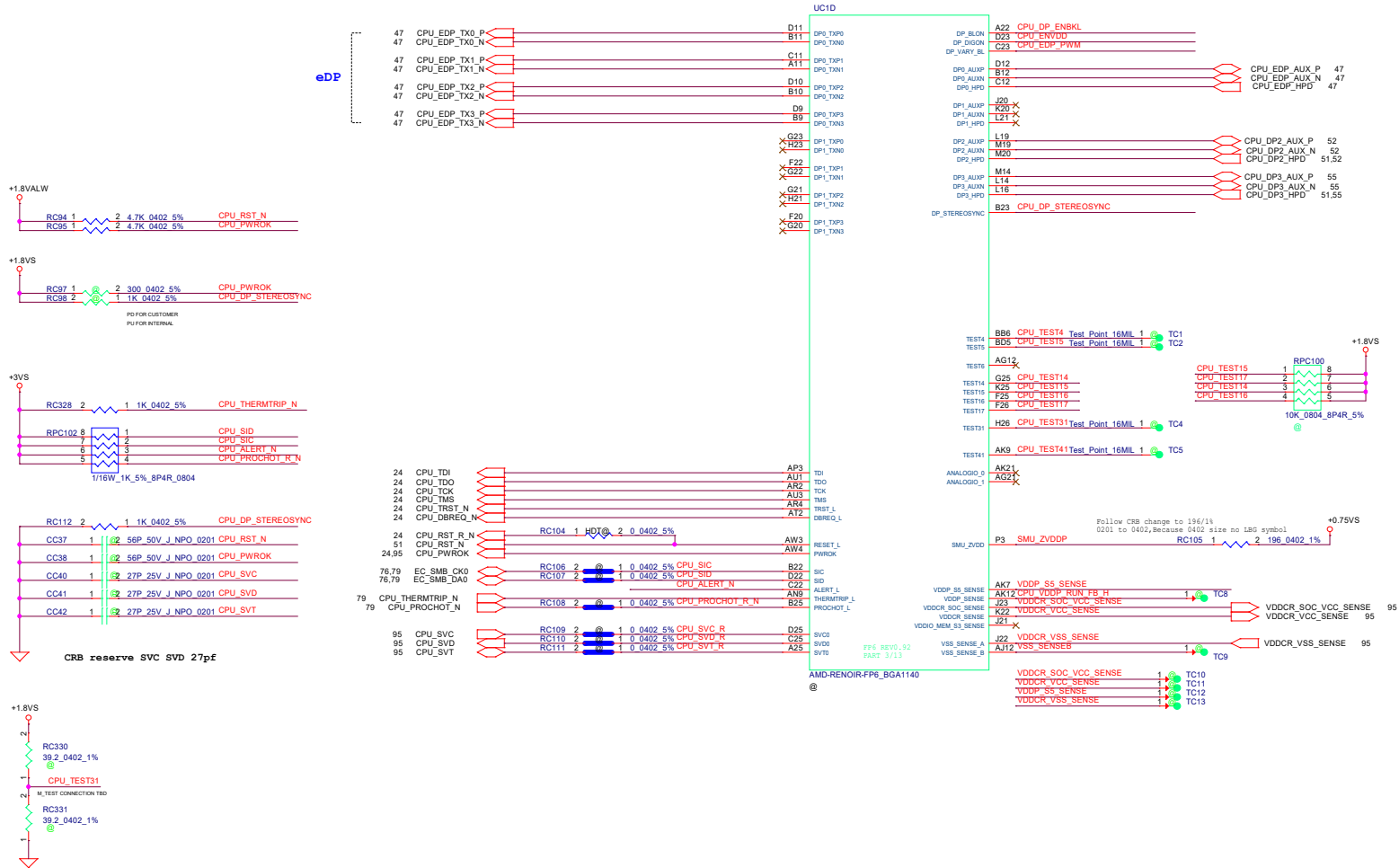
PCH ISH I2C0 address

Device	Address
TOF	
Accelerometer(MB)	001 1000b
Accelerometer(DB)	001 1001b
Light Sensor	1000 100xb

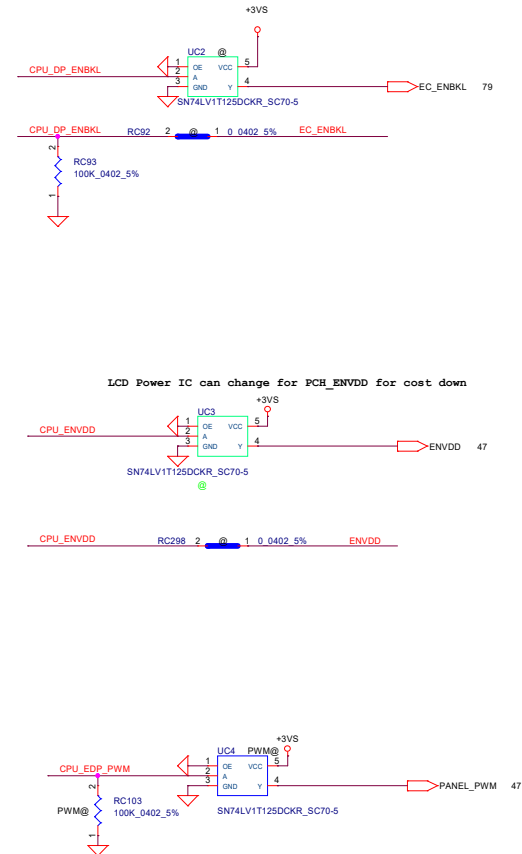
EC SMBus4 address

Device	Address
PD	TBD

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C				C																													
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A				A																													
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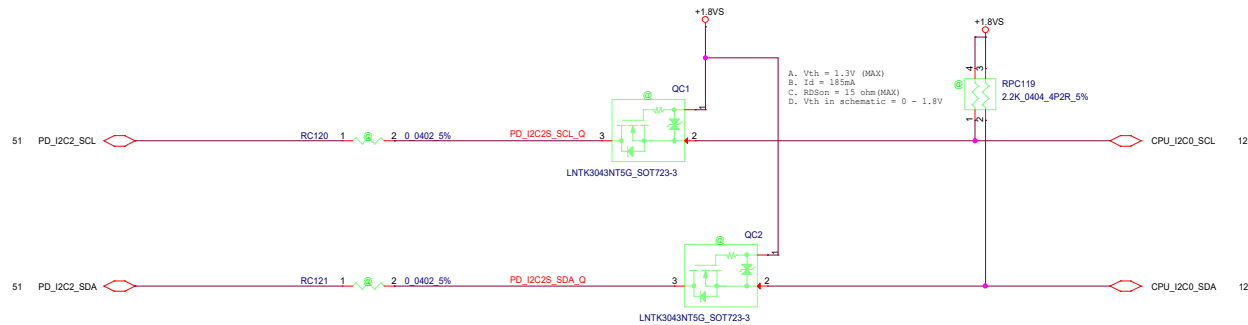


To EDP panel



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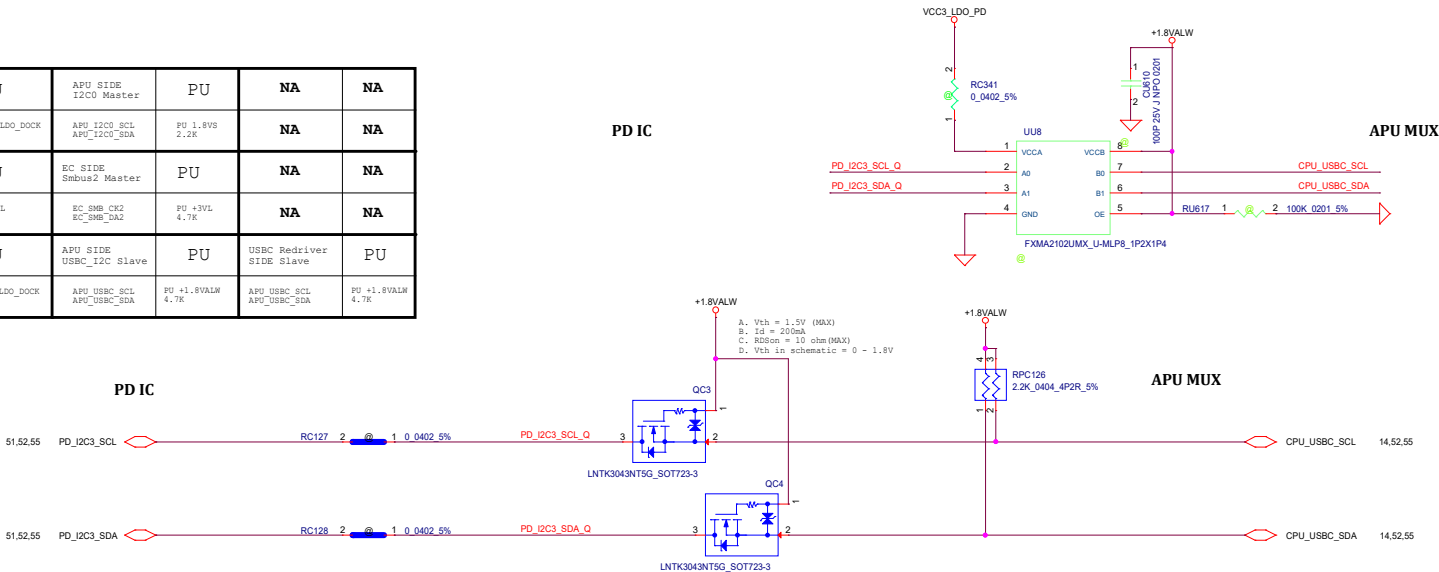
PD FW Update



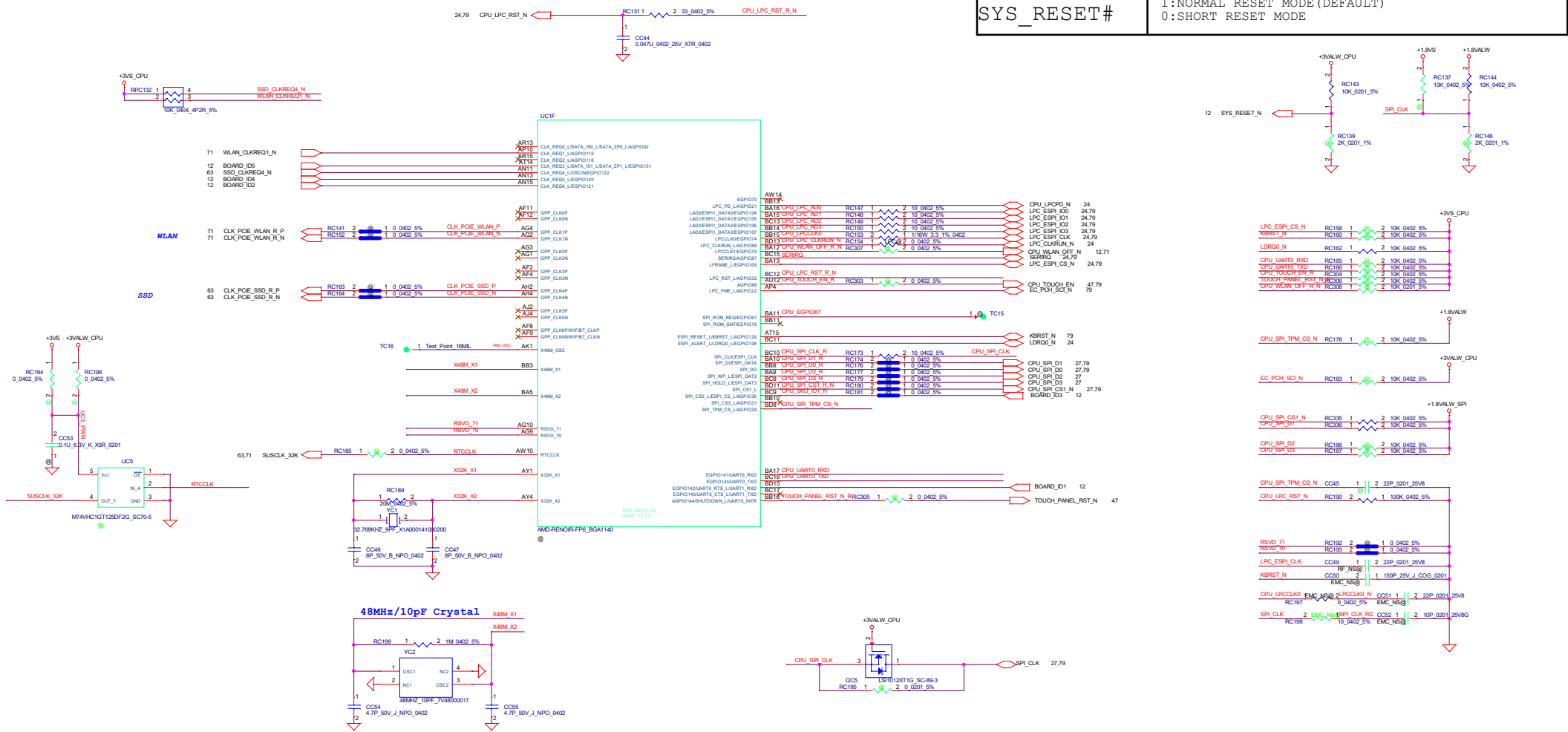
此table注意要更新

I2C1	Level Shift	PD SIDE I2C1 Slave	PU	APU SIDE I2C0 Master	PU	NA	NA
PD update FW	QC50 QC51	PD_I2C1_SCL PD_I2C1_SDA	PU VCC3_LDO_DOCK 4.7K	APU_I2C0_SCL APU_I2C0_SDA	PU 1.8VS 2.2K	NA	NA
I2C2	Level Shift	PD SIDE I2C2 Slave	PU	EC SIDE Smbus2 Master	PU	NA	NA
PD to EC	NA	PD_I2C2_SCL_R PD_I2C2_SDA_R	PU +3VL 4.7K	EC_SMB_CK2 EC_SMB_DAA2	PU +3VL 4.7K	NA	NA
I2C3	Level Shift	PD SIDE I2C3 Master	PU	APU SIDE USBC_I2C Slave	PU	USBC Redriver SIDE Slave	PU
PD for USBC redriver and APU Mux	QC14 QC5	PD_I2C3_SCL_R PD_I2C3_SDA_R	PU VIP8_LDO_DOCK 4.7K	APU_USBC_SCL APU_USBC_SDA	PU +1.8VALW 4.7K	APU_USBC_SCL APU_USBC_SDA	PU +1.8VALW 4.7K

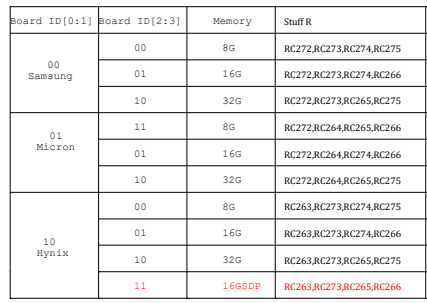
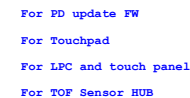
PD for USBC redriver and APU Mux



STRAP PINS	SYS_RESET#
PCH_SPI_CLK	1:USE 48MHZ CRYSTAL CLOCK AND GENERATE BOTH INTERNAL AND EXTERNAL CLOCKS (DEFAULT) 0:USE 100MHZ PCIE CLOCK AS REFERENCE CLOCK AND GENERATE INTERNAL CLOCKS ONLY
SYS_RESET#	1:NORMAL RESET MODE (DEFAULT) 0:SHORT RESET MODE



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IDO	AGPIO130	S0_3.3V
ID1	EGPIO142	S0_3.3V
ID2	EGPIO121	S0_3.3V
ID3	AGPIO30	+1.8VALW

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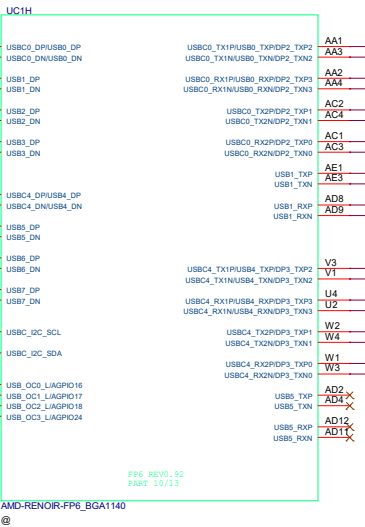
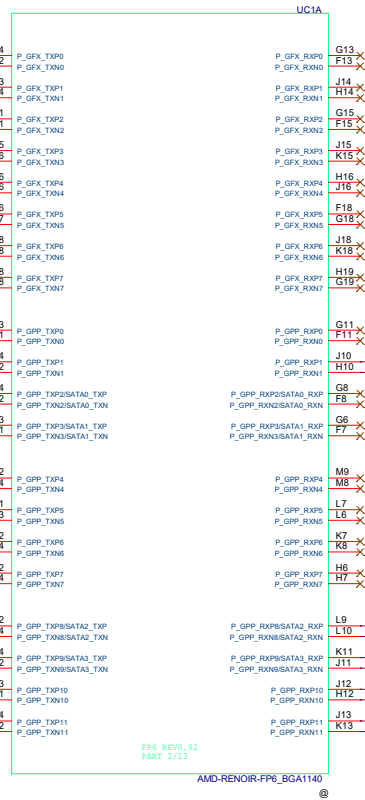
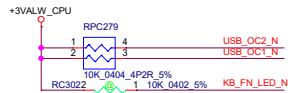
WLAN

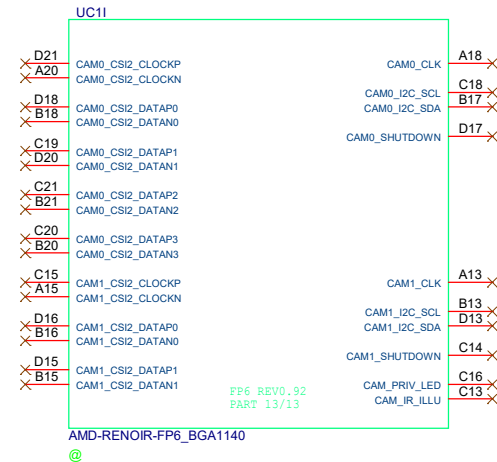
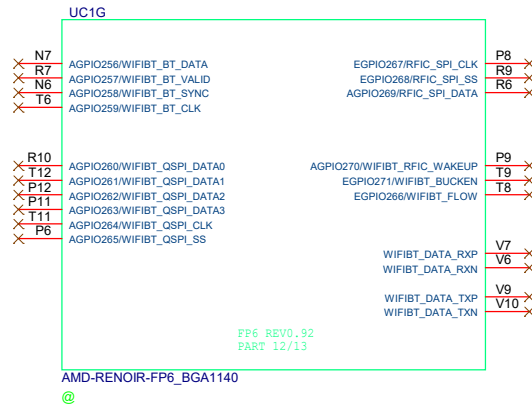
SSD

TYPE C 1 W/DP
TYPE A AOU
Camera

TYPE C 2 W/DP

BT

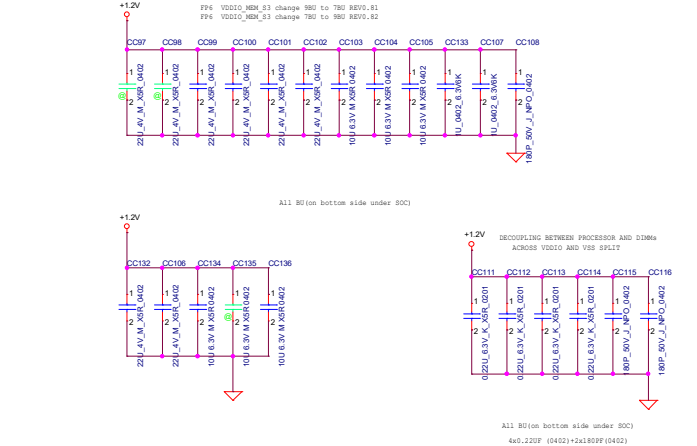
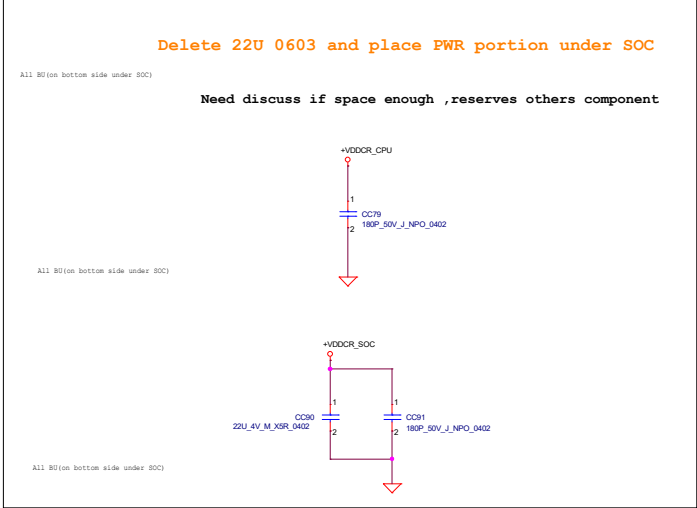
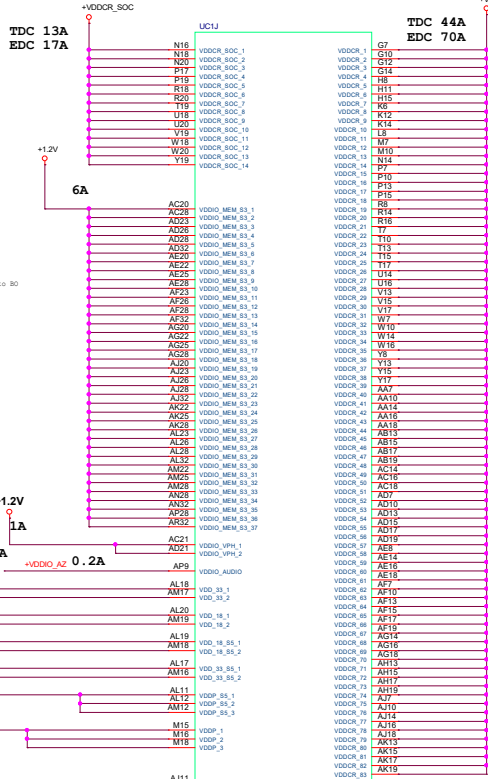
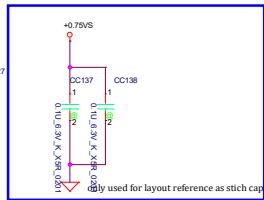
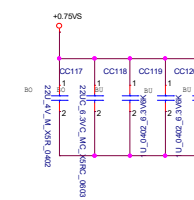
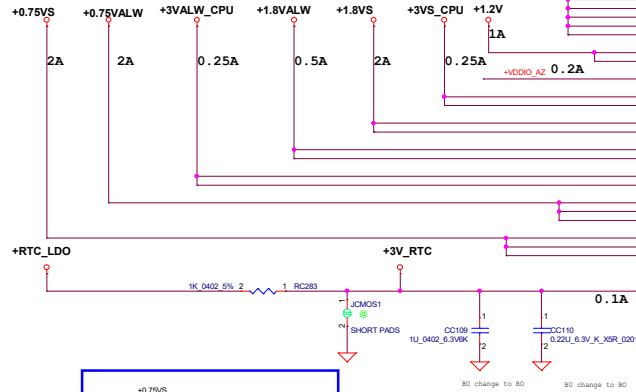
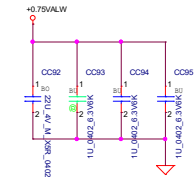
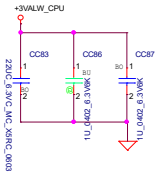
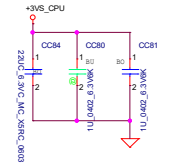
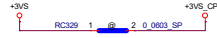
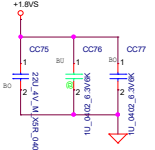
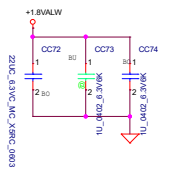





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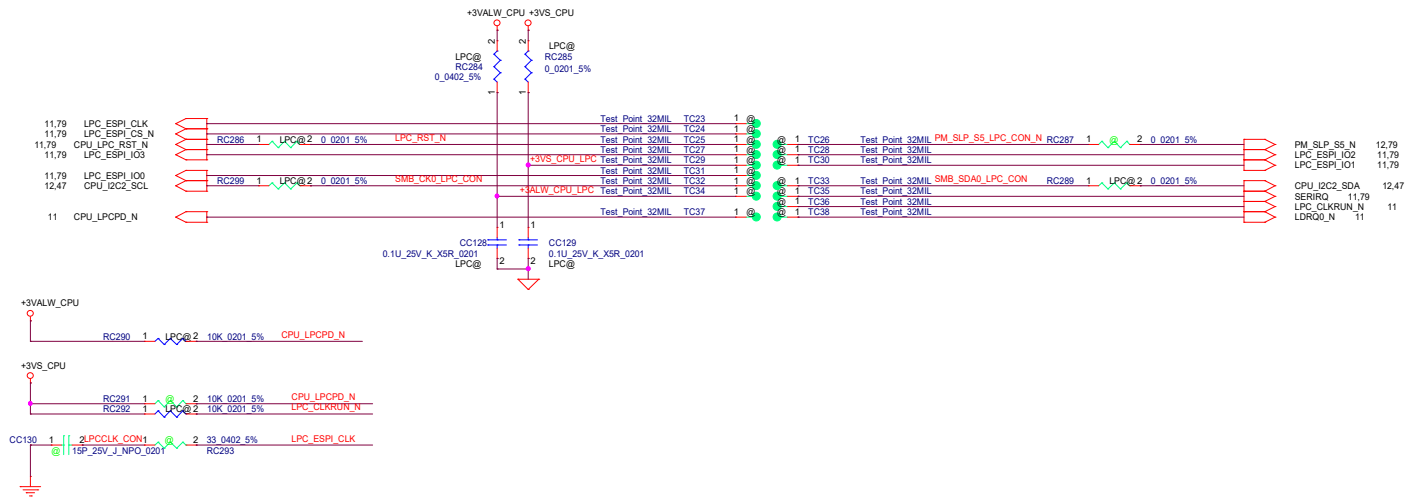
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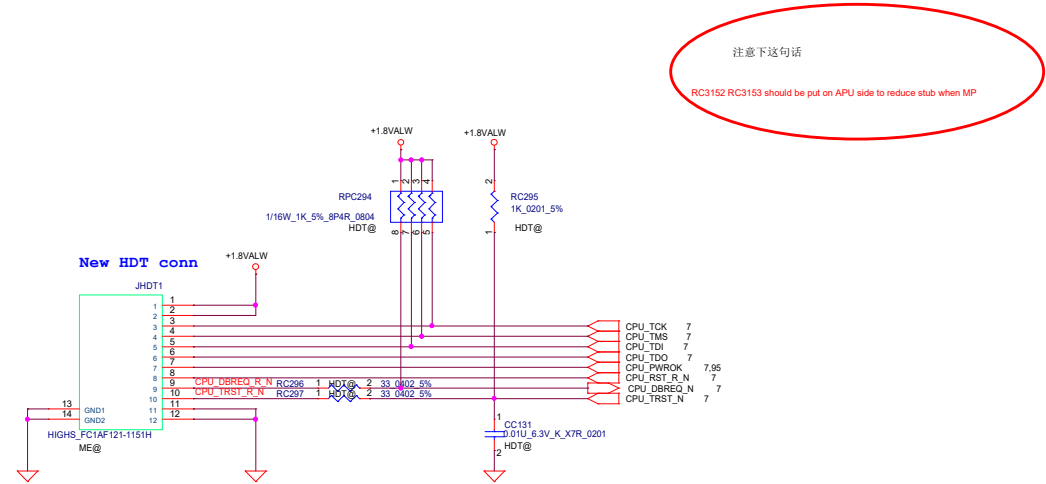
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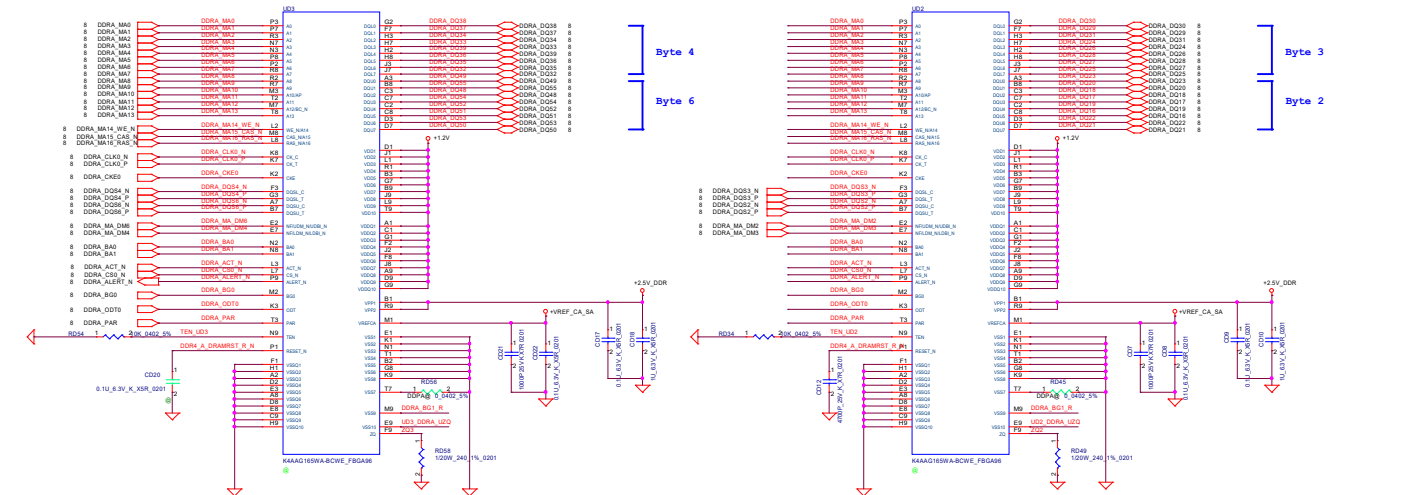
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LPC ROM EMULATOR HEADER

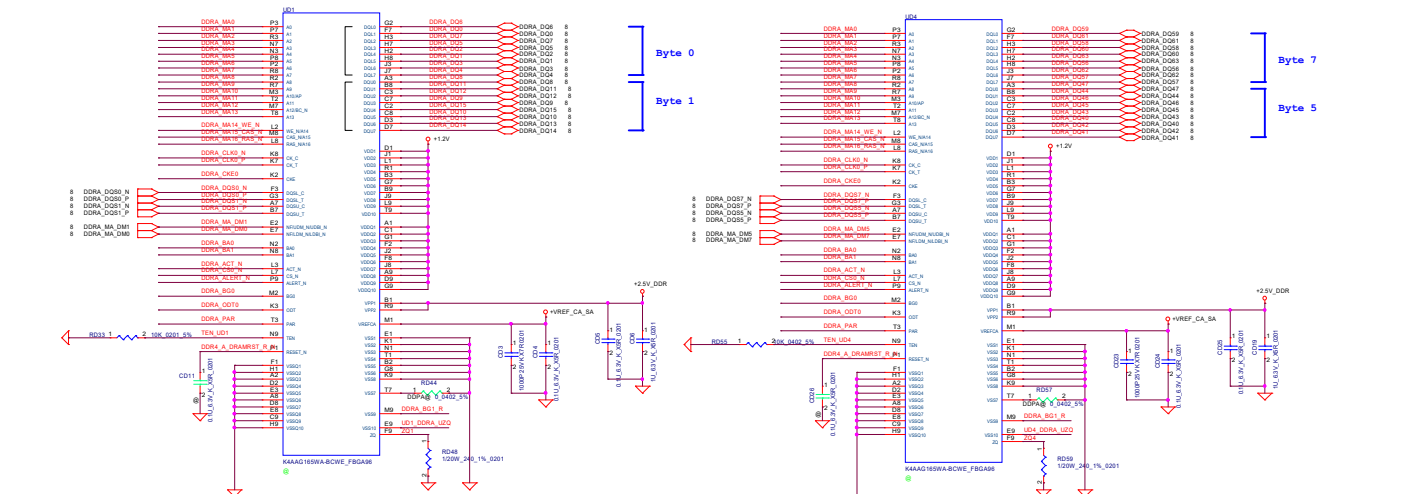


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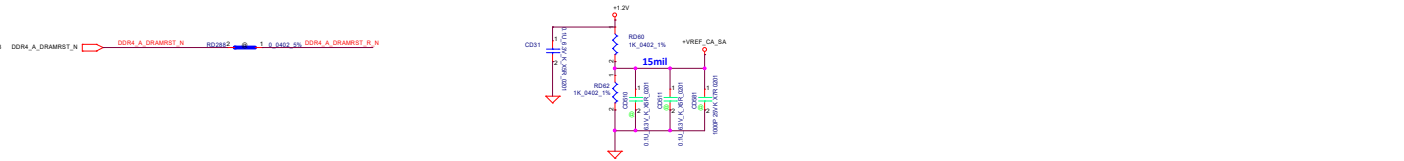
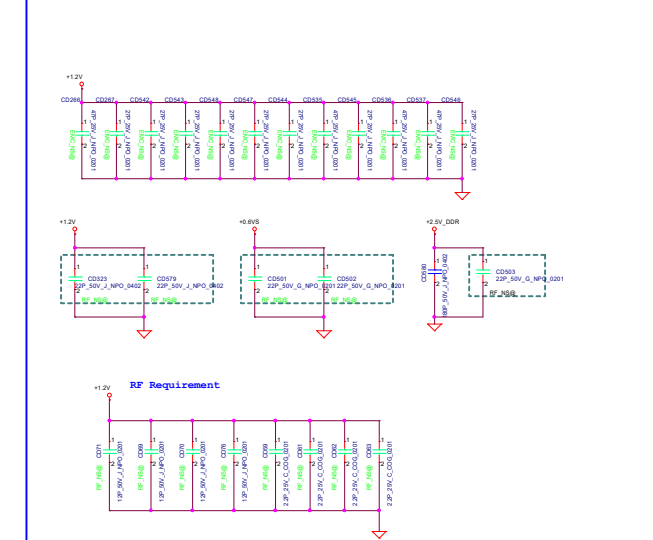




Note: The memory GSD signal pairs are routed point to point and reference either the 100 plane or the 10010_001_001 plane. The GSD termination must match the GSD reference plane



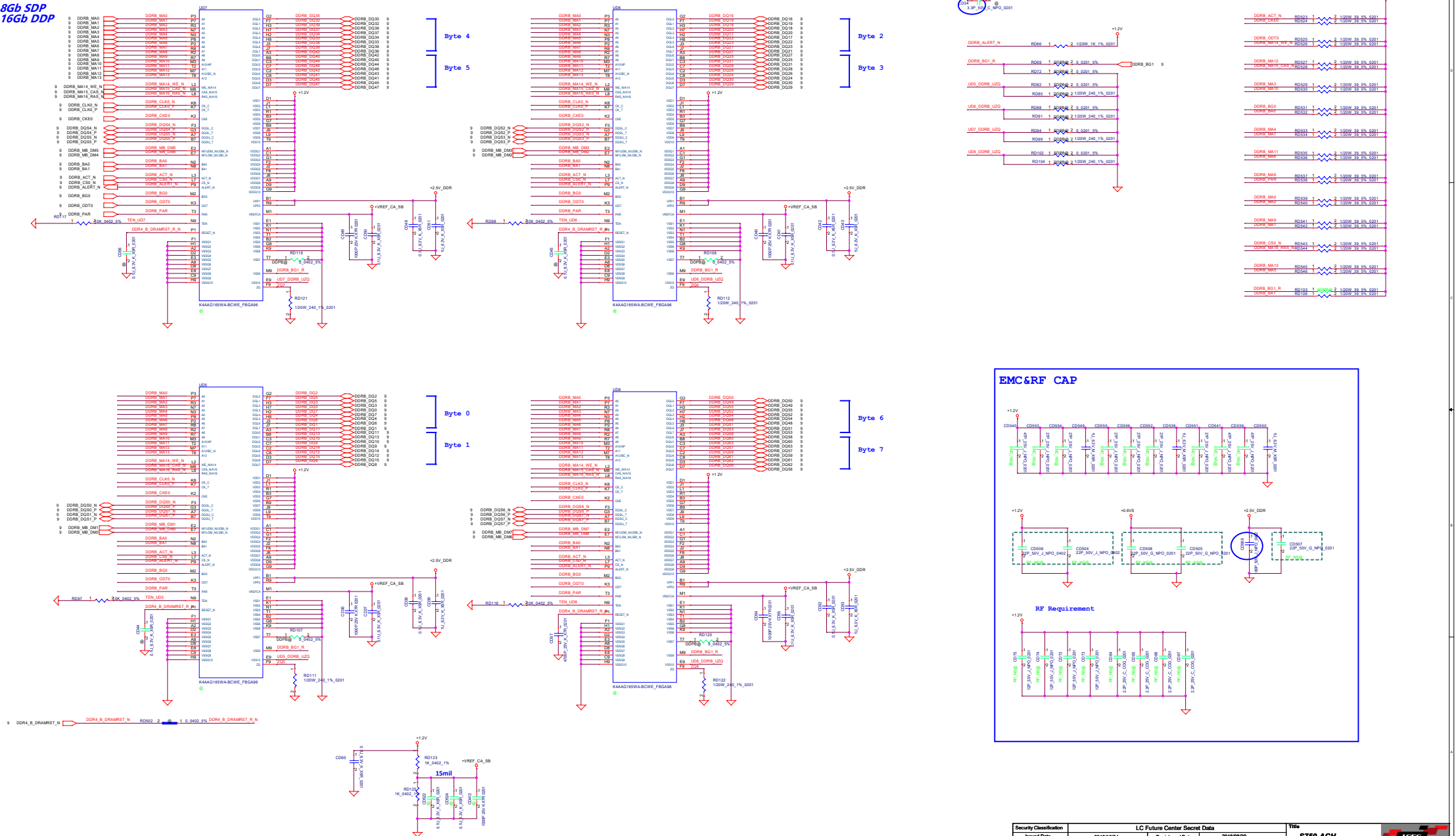
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8Gb SDP
16Gb DDP



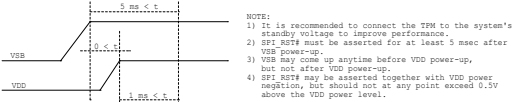
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TPM RESET

TPM

TABLE of TPM (U9801)		
Vendor	P/N	LCFC P/N
Nuvoton	NPCT750LABYX	SA00008KS20
ST Micro	ST33HTPH2E32AHC0	SA000089E20

NOTE:
Check timing sequence in SDV phase.



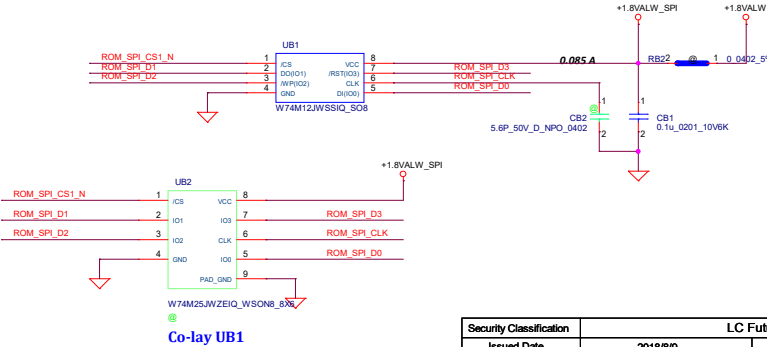
TABLE


Pin No	TCG PTP Spec (v38)	Nuvoton NPCT750LABYX	ST Micro ST33HTPH2E32AHC0
1	VDD	VSB	NC
2	GND	NC	GND
3	NC	NC	NC
4	GPIO	GPIO/PP	PP
5	NC	NC	NC
6	GPIO	GPIO3	NC
7	GPIO	NC	GPIO
8	VDD	VHIO	NC
9	NC	NC	NC
10	NC	NC	NC
11	NC	NC	NC
12	NC	NC	NC
13	GPIO	GPIO4	NC
14	NC	NC	NC
15	NC	NC	NC
16	GND	GND	NC
17	SPI_RST#	RST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#/GPIO2	SPI_PIRQ#
19	SPI_CLK	SCLK	SPI_CLK
20	SPI_CS#	SCS#/GPIO5	SPI_CS#
21	MOSI	MOSI/GPIO7	MOSI
22	VDD	VHIO	VPS
23	GND	GND	NC
24	MISO	MISO	MISO
25	NC	NC	NC
26	NC	NC	NC
27	NC	NC	NC
28	NC	NC	NC
29	SDA/GPIO1	SDA/GPIO1	NC
30	SDA/GPIO0	SDA/GPIO0	NC
31	NC	NC	NC
32	NC	NC	NC

SPI ROM

Used RPM BIOS ROM

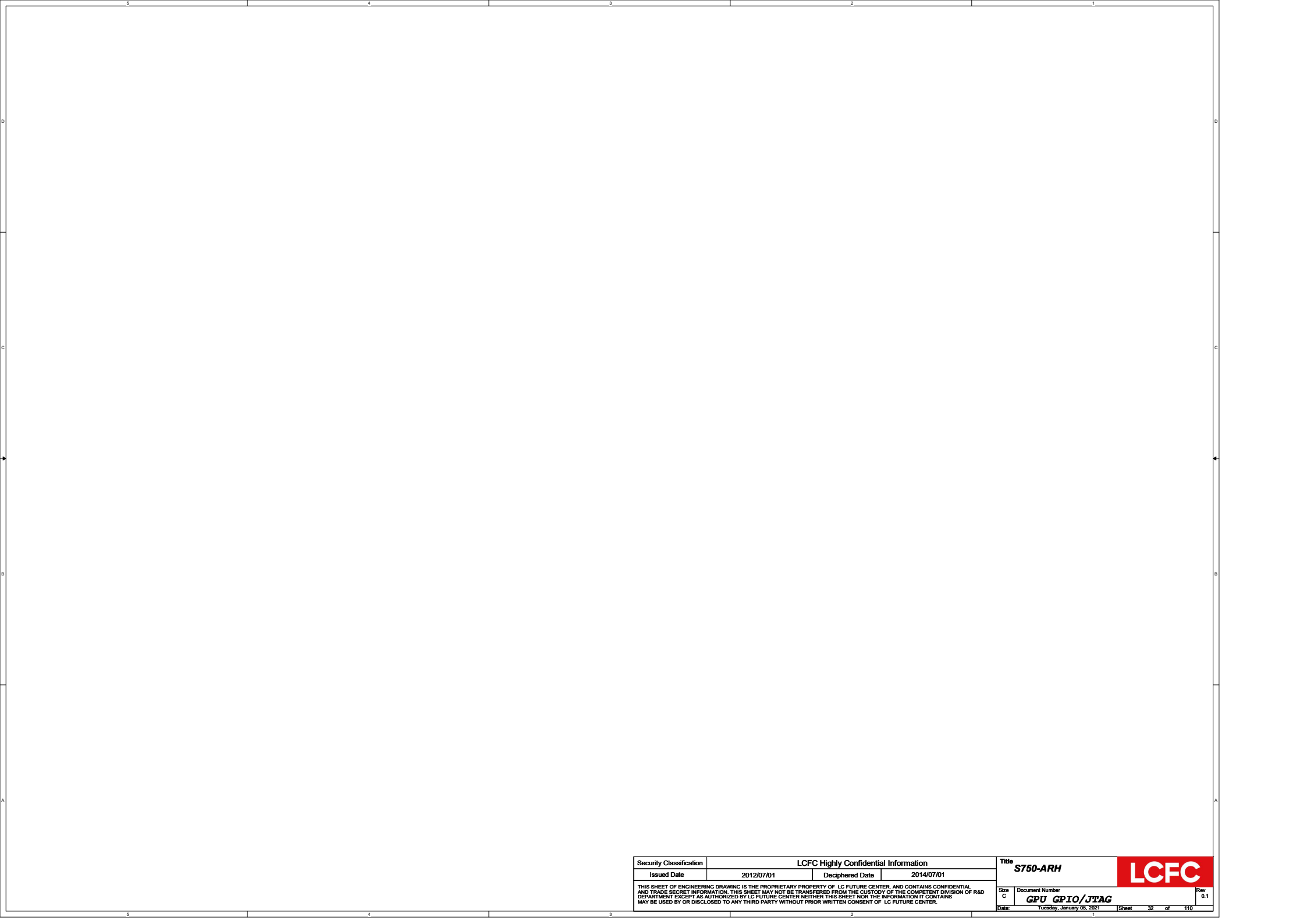
11.79	CPU_SPI_CS1_N	RB13	2	0	1	0.0402	5%	ROM_SPI_CS1_N
11.79	CPU_SPI_D0	RB11	2	1	0	0.0402	5%	ROM_SPI_D0
11.79	CPU_SPI_D1	RB12	2	0	1	0.0402	5%	ROM_SPI_D1
11.79	SPI_CLK	RB10	2	0	1	0.0402	5%	ROM_SPI_CLK
11	CPU_SPI_D2	RB21	2	0	1	0.0402	5%	ROM_SPI_D2
11	CPU_SPI_D3	RB22	2	0	1	0.0402	5%	ROM_SPI_D3



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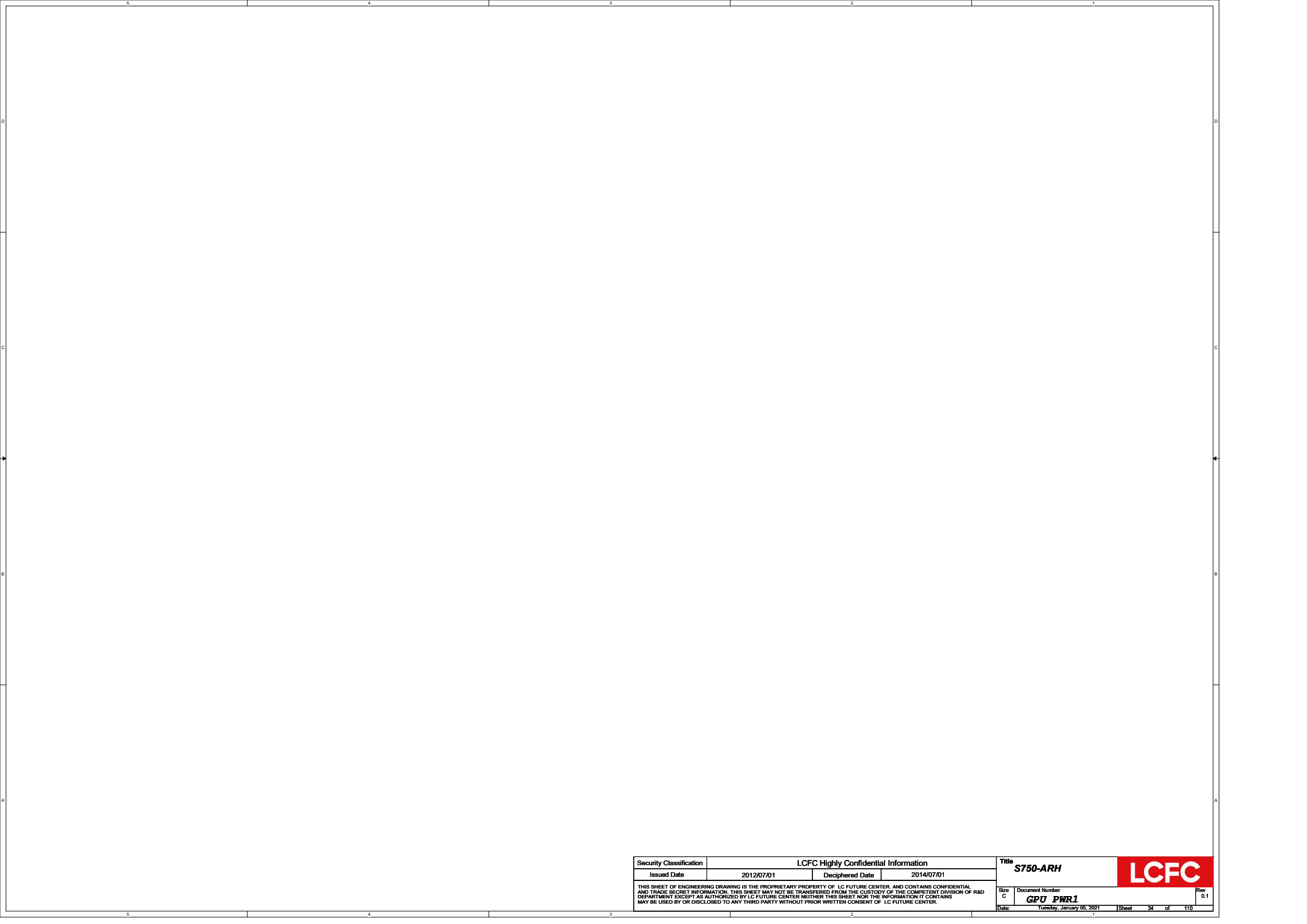
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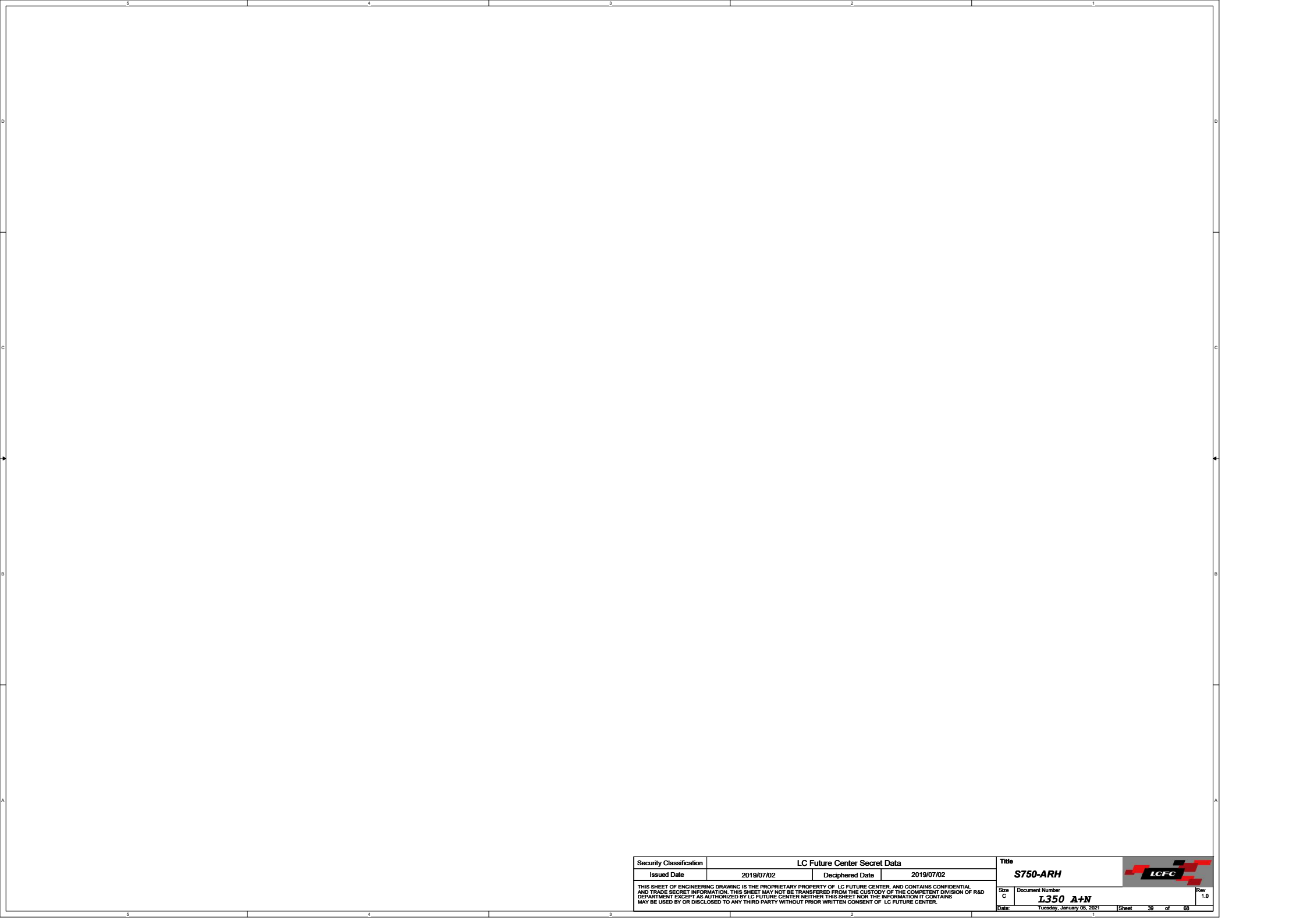






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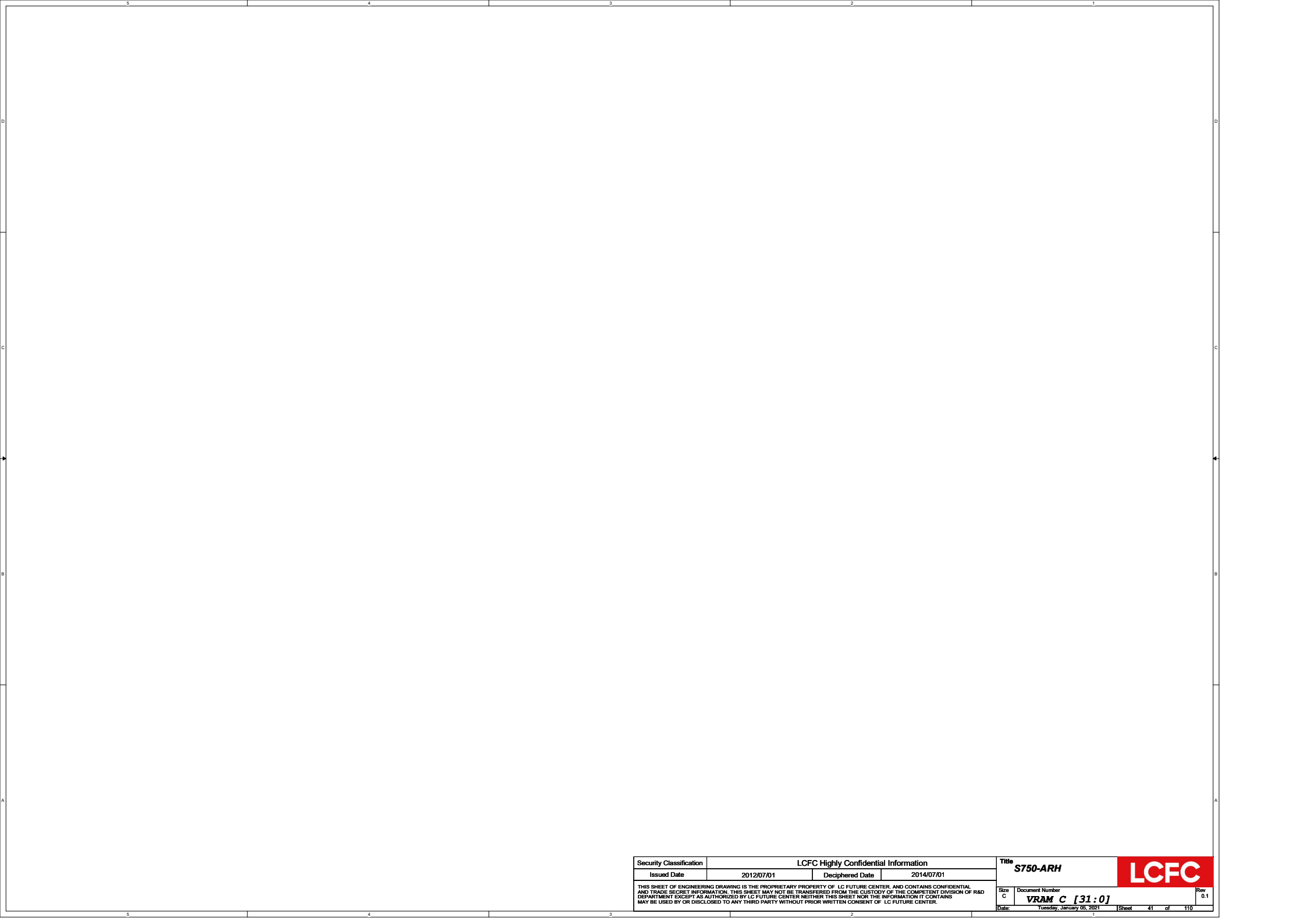
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<div><table><tr><td>Security Classification</td><td colspan="3">LC Future Center Secret Data</td><td>Title</td></tr><tr><td>Issued Date</td><td>2019/07/02</td><td>Deciphered Date</td><td>2019/07/02</td><td>S750-ARH</td></tr><tr><td colspan="4">THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.</td><td><div><div>Size C</div><div>Document Number L350 A+N</div><div>Date Tuesday, January 05, 2021</div></div><div><div>Rev 1.0</div><div>Sheet 38 of 88</div></div></td></tr></table></div>					Security Classification	LC Future Center Secret Data			Title	Issued Date	2019/07/02	Deciphered Date	2019/07/02	S750-ARH	THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				<div><div>Size C</div><div>Document Number L350 A+N</div><div>Date Tuesday, January 05, 2021</div></div> <div><div>Rev 1.0</div><div>Sheet 38 of 88</div></div>
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Size	Document Number			Rev	
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				C	VRAM C [31:0]	0.1	
				Date:	Tuesday, January 05, 2021	Sheet	41 of 110

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					Date:	Tuesday, January 05, 2021	Sheet 42 of 110

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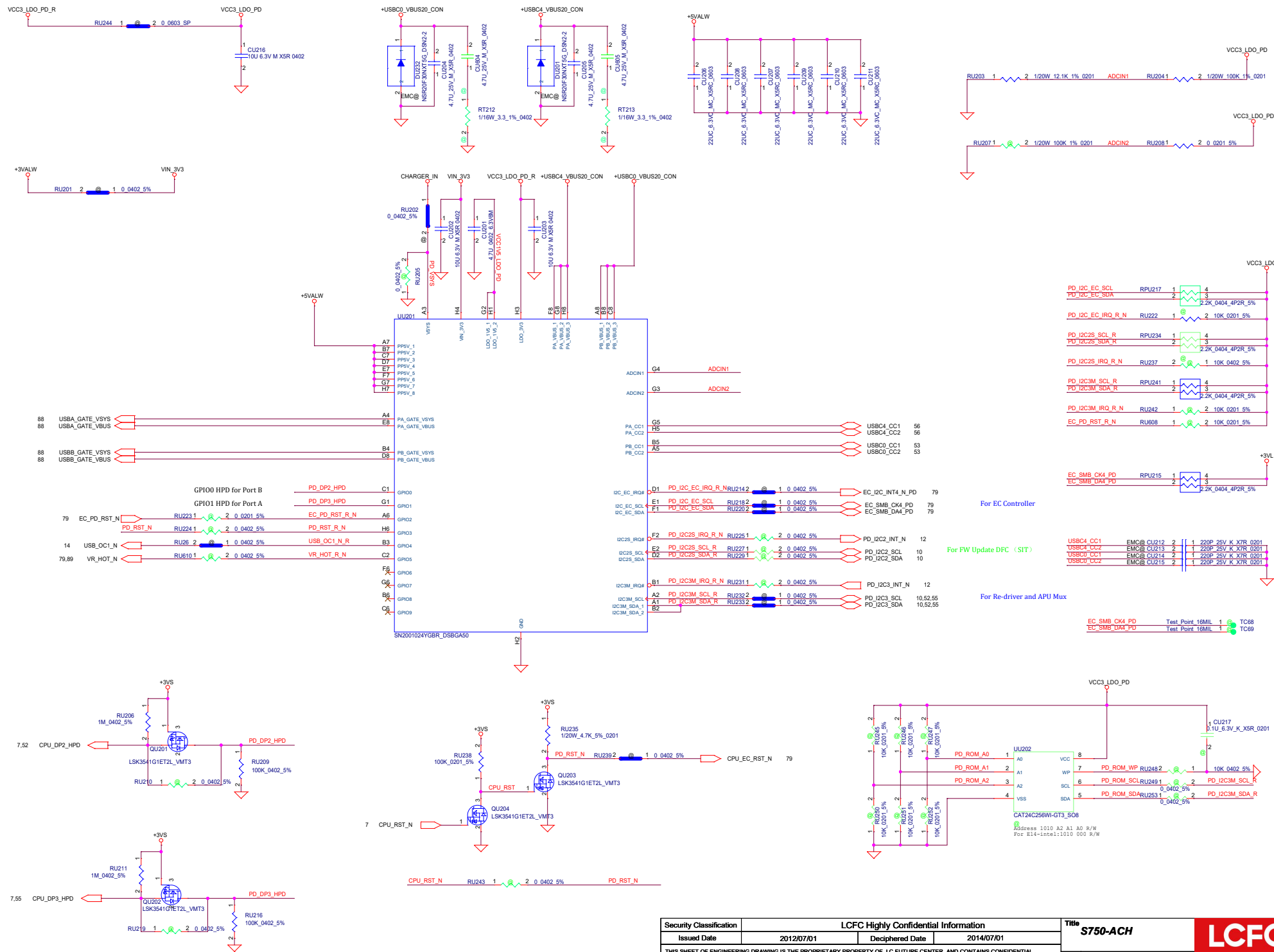
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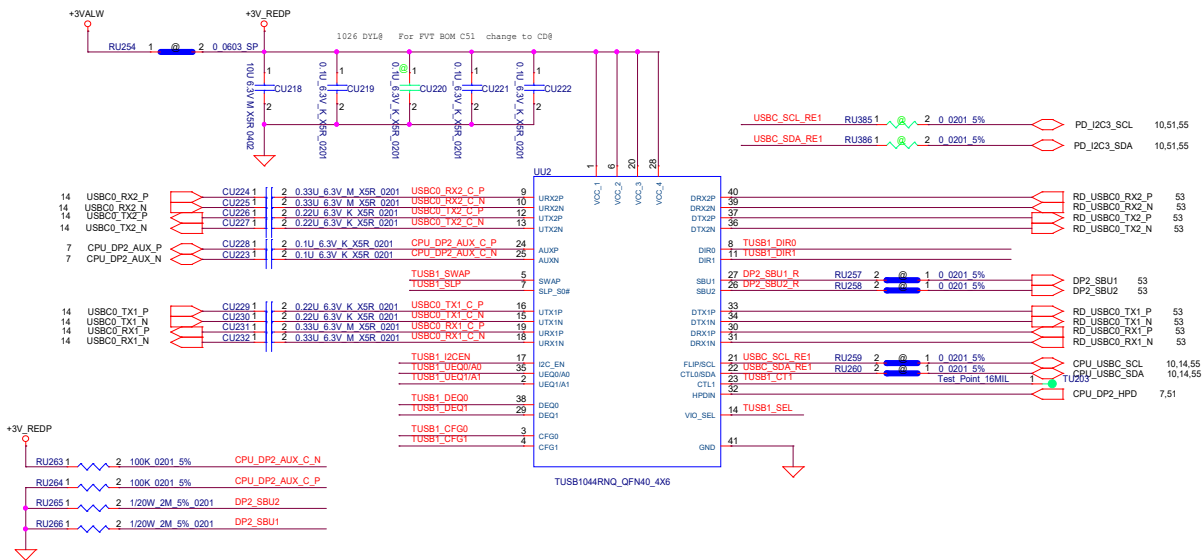
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				Date:	Tuesday, January 05, 2021	Sheet 43 of 110

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				Sheet 44 of 110																									
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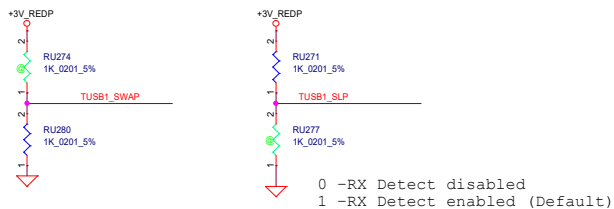
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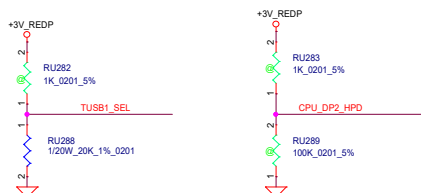


0 - Do not swap channel directions and EQ settings (Default)
1 - Swap channel directions and EQ settings

Will change to unstuff!!!

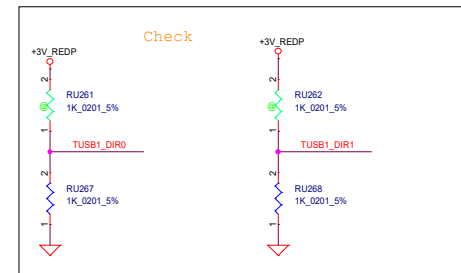


0 -RX Detect disabled
1 -RX Detect enabled (Default)

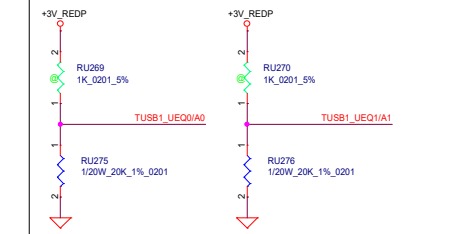


0 option1: Tie 1K 5% to GND option2: Tie directly to GND
R Tie to 20K 5% to GND
F Float (leave PIN open)
1 option1: Tie 1K 5% to VCC option2: Tie directly to VCC

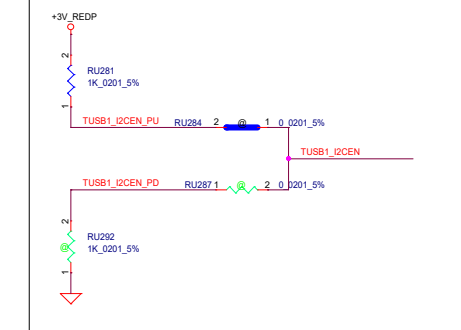
This PIN selects I/O voltage levels for the 2-level GPIO and I2C
0 = 3.3-V configuration I/O voltage, 3.3-V I2C interface (Default)
R = 3.3-V configuration I/O voltage, 1.8-V I2C interface
F = 1.8-V configuration I/O voltage, 3.3-V I2C interface
1 = 1.8-V configuration I/O voltage, 1.8-V I2C interface



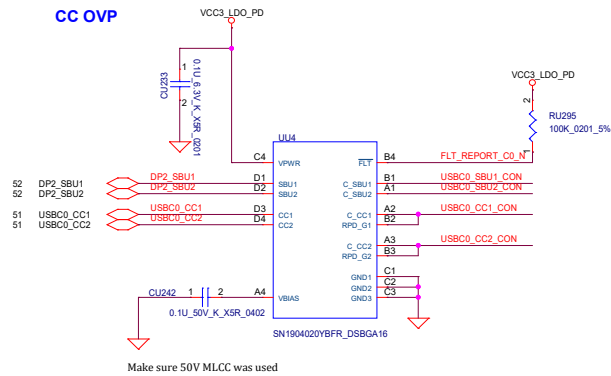
Address 00



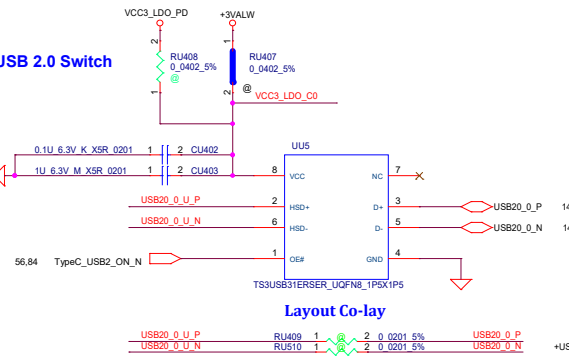
I2C_EN=0 GPIO MODE
I2C_EN=1 I2C enable



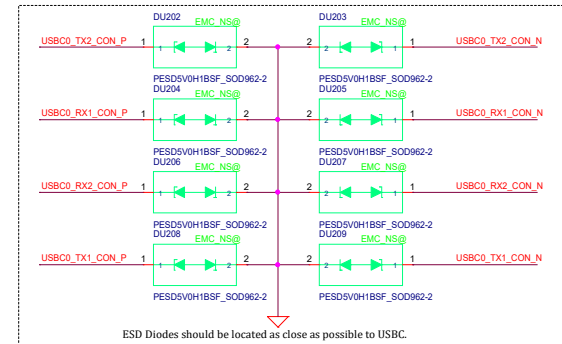
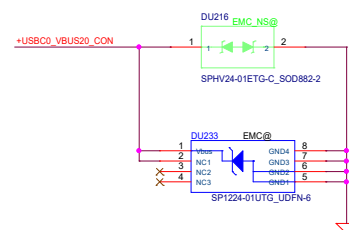
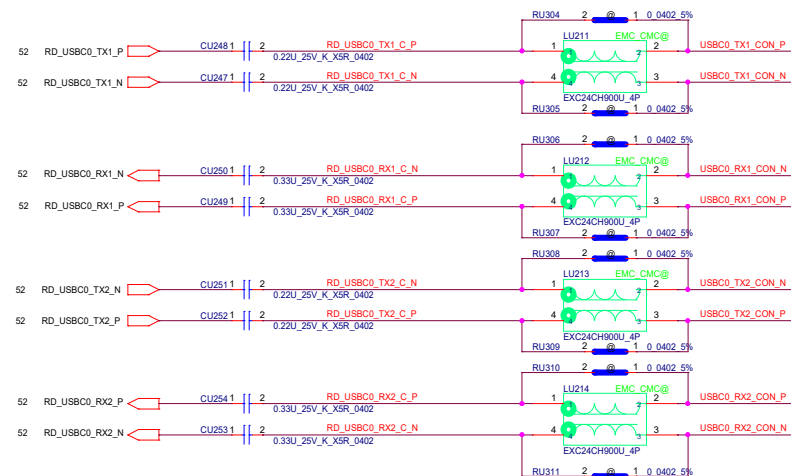
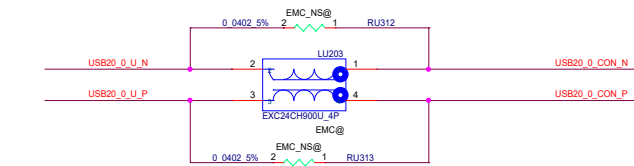
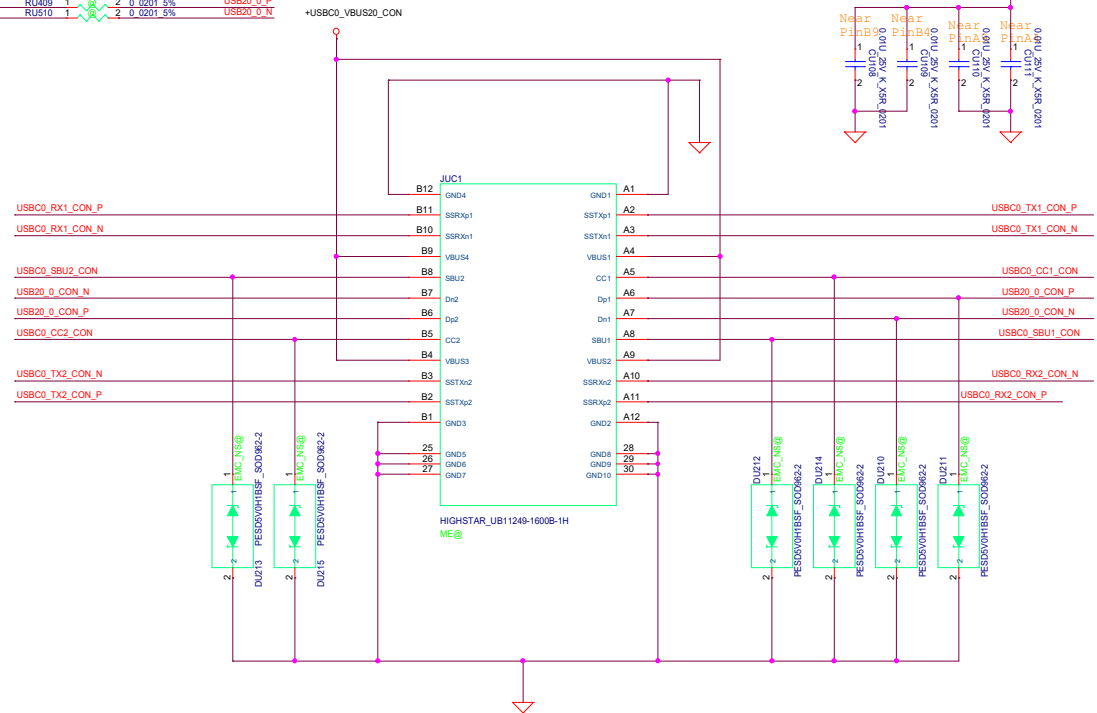
CC OVP



USB 2.0 Switch



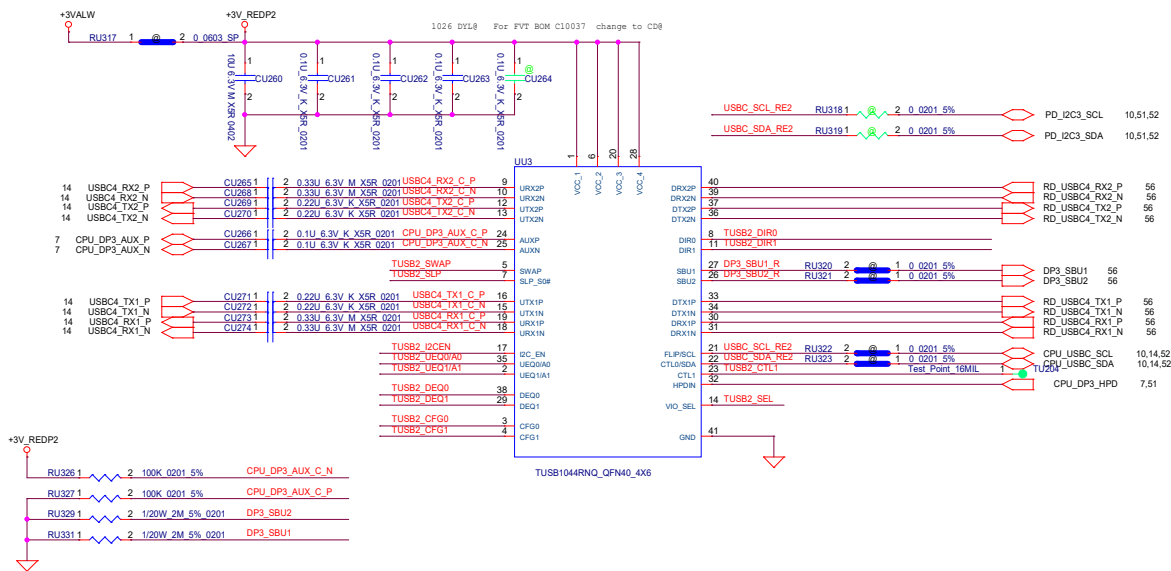
Layout Co-lay



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Size C		Document Number						Rev 0.1	
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Date:		(uesday, January 05, 2021)						Sheet 53 of 110	

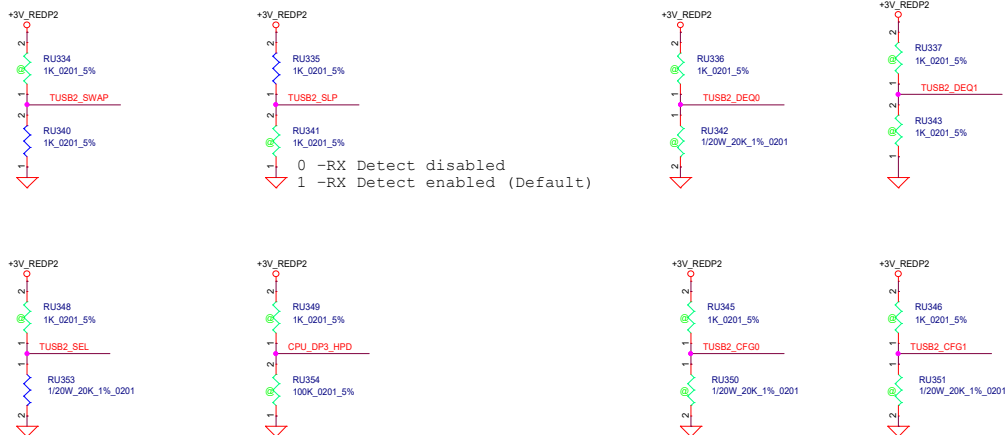
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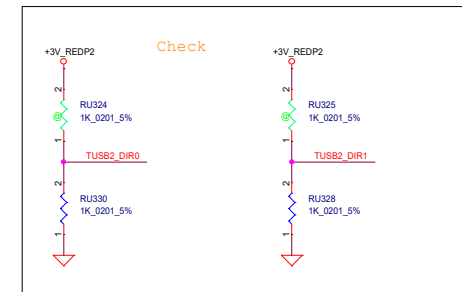
0 - Do not swap channel directions and EQ settings (Default)
1 - Swap channel directions and EQ settings

EQ setting

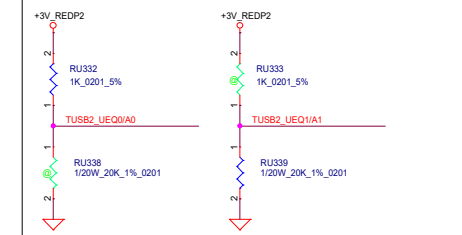


0 option1: Tie 1K 5% to GND option2: Tie directly to GND
R Tie to 20K 5% to GND
F Float (leave pin open)
1 option1: Tie 1K 5% to VCC option2: Tie directly to VCC

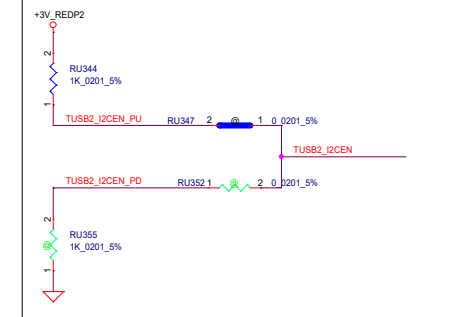
This PIN selects I/O voltage levels for the 2-level GPIO and I2C
0 = 3.3-V configuration I/O voltage, 3.3-V I2C interface (Default)
R = 3.3-V configuration I/O voltage, 1.8-V I2C interface
F = 1.8V configuration I/O voltage, 3.3-V I2C interface
1 = 1.8-V configuration I/O voltage, 1.8-V I2C interface



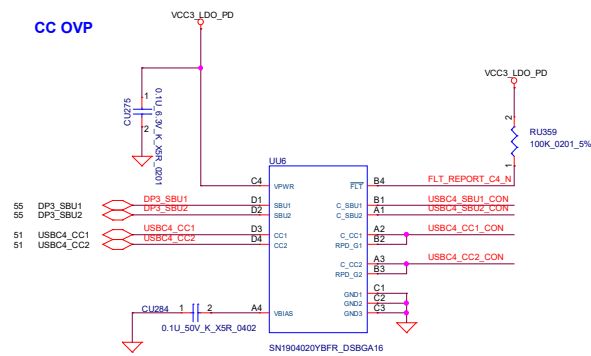
Address 01



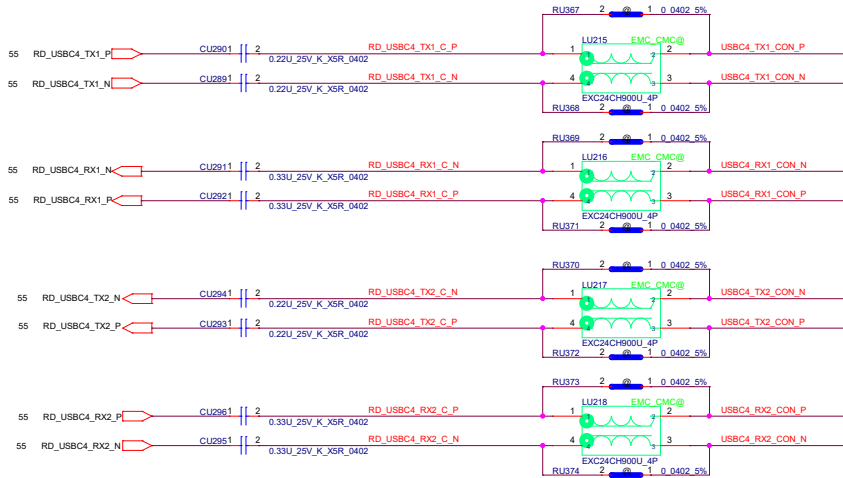
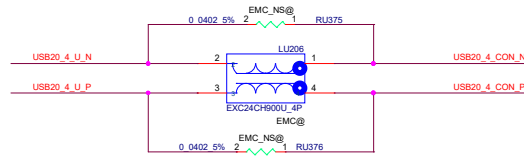
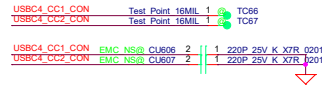
I2C_EN=0 GPIO MODE I2C_EN=1 I2C enable



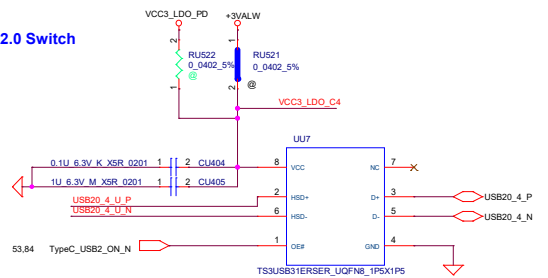
CC OVP



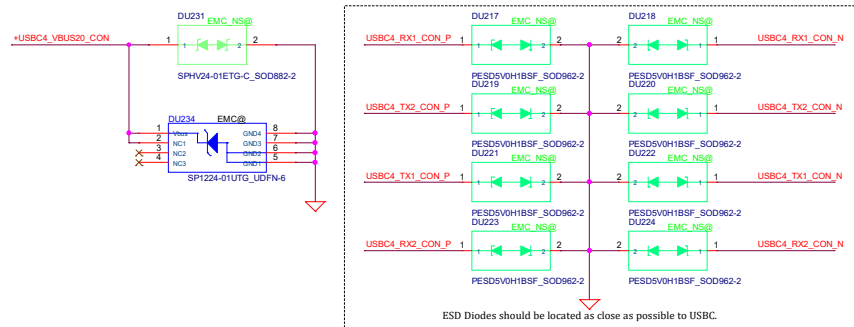
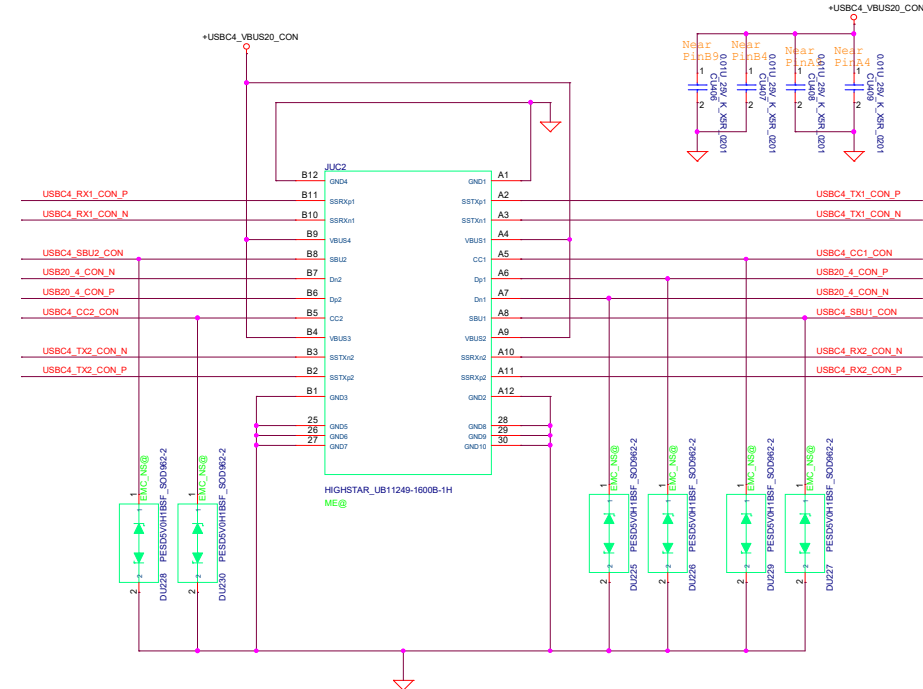
Make sure 50V MLCC was used



USB 2.0 Switch



Layout Co-ly



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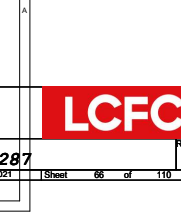
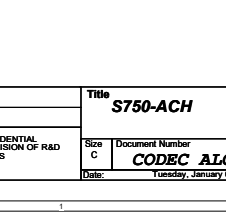
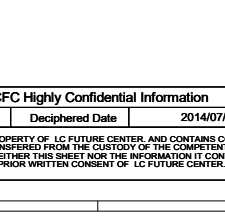
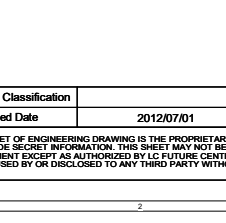
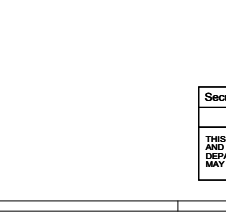
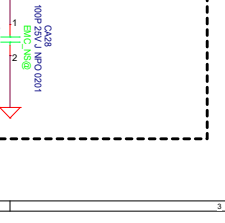
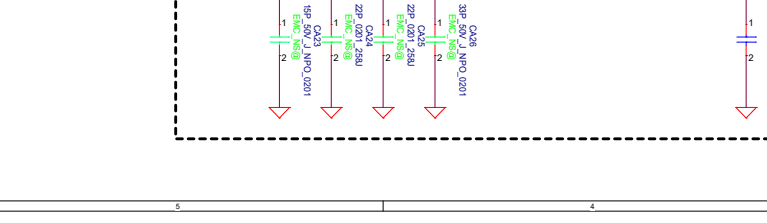
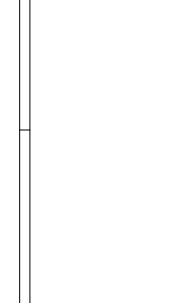
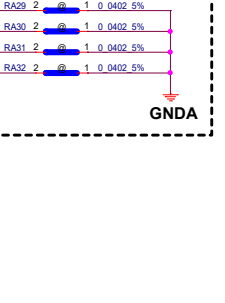
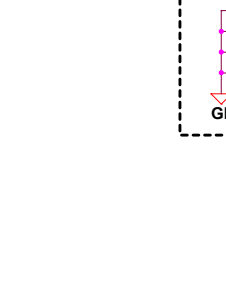
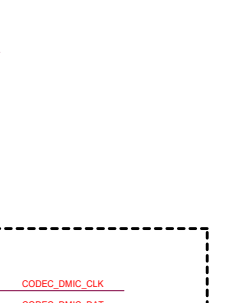
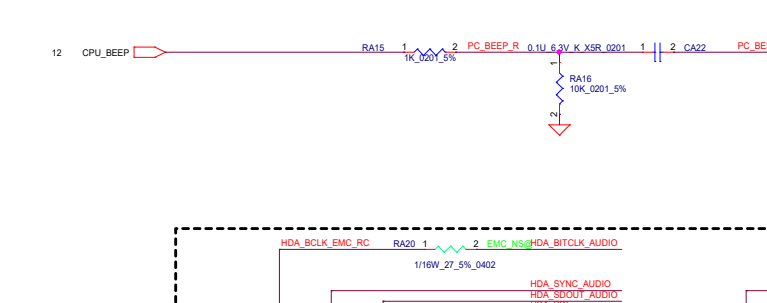
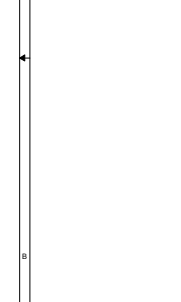
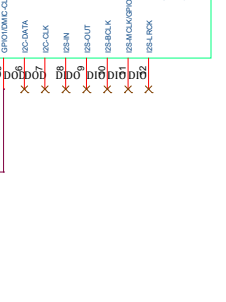
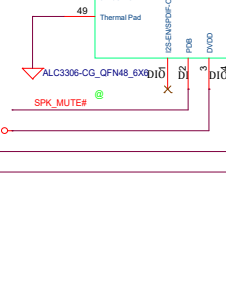
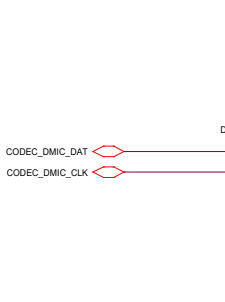
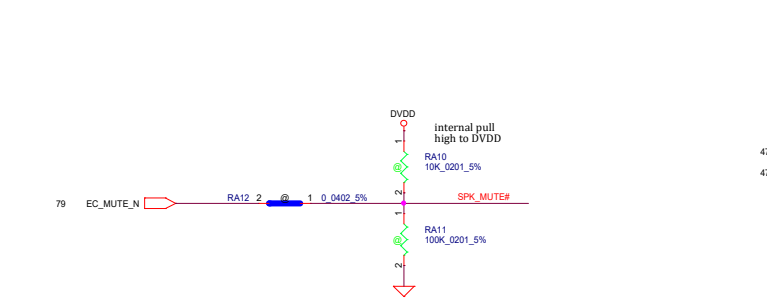
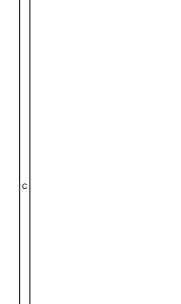
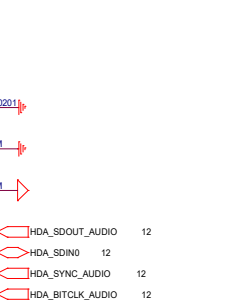
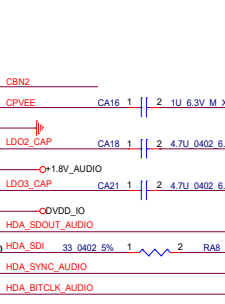
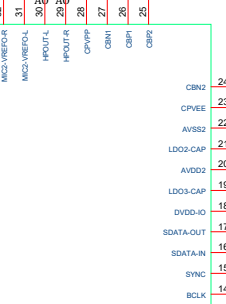
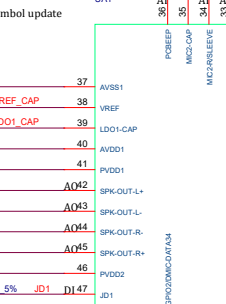
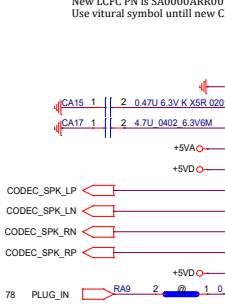
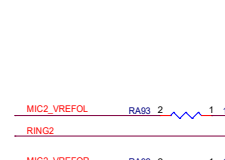
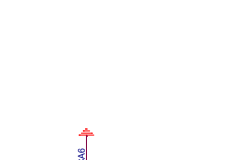
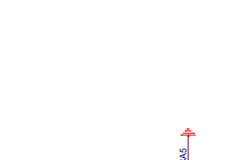
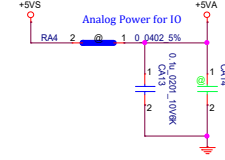
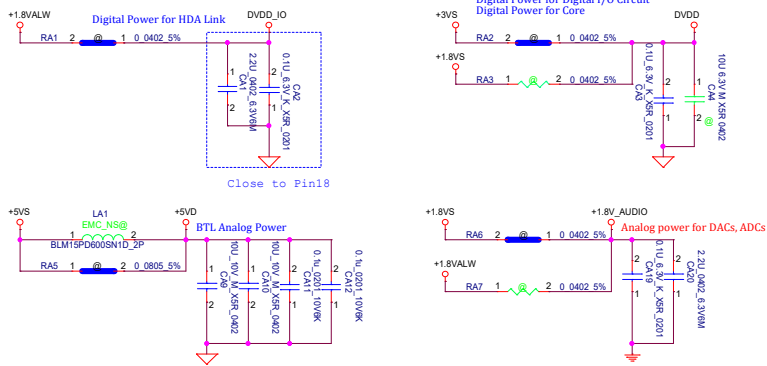




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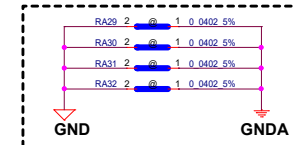
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Vendor update MPN to ALC3306-VA1-CG
New LCFC PN is SA0000ARR00
Use vitural symbol untill new CIS symbol update

Codec Only



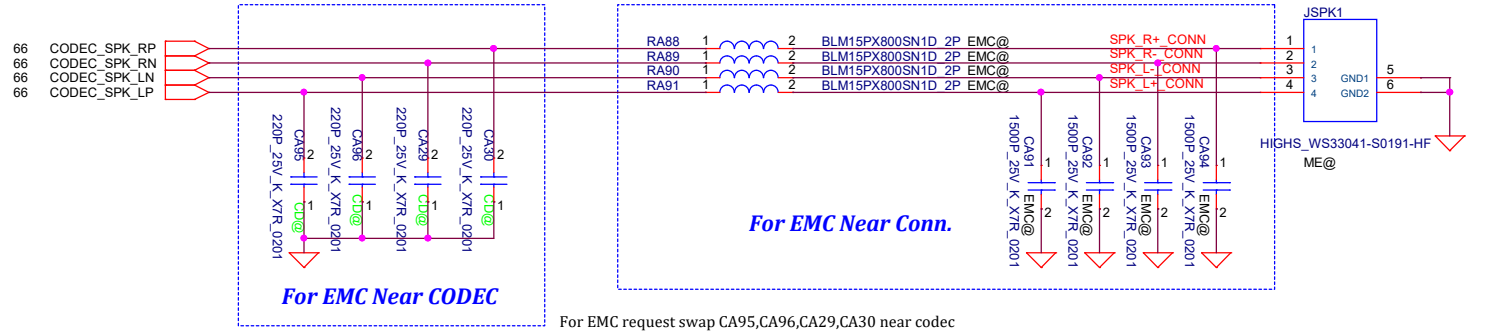
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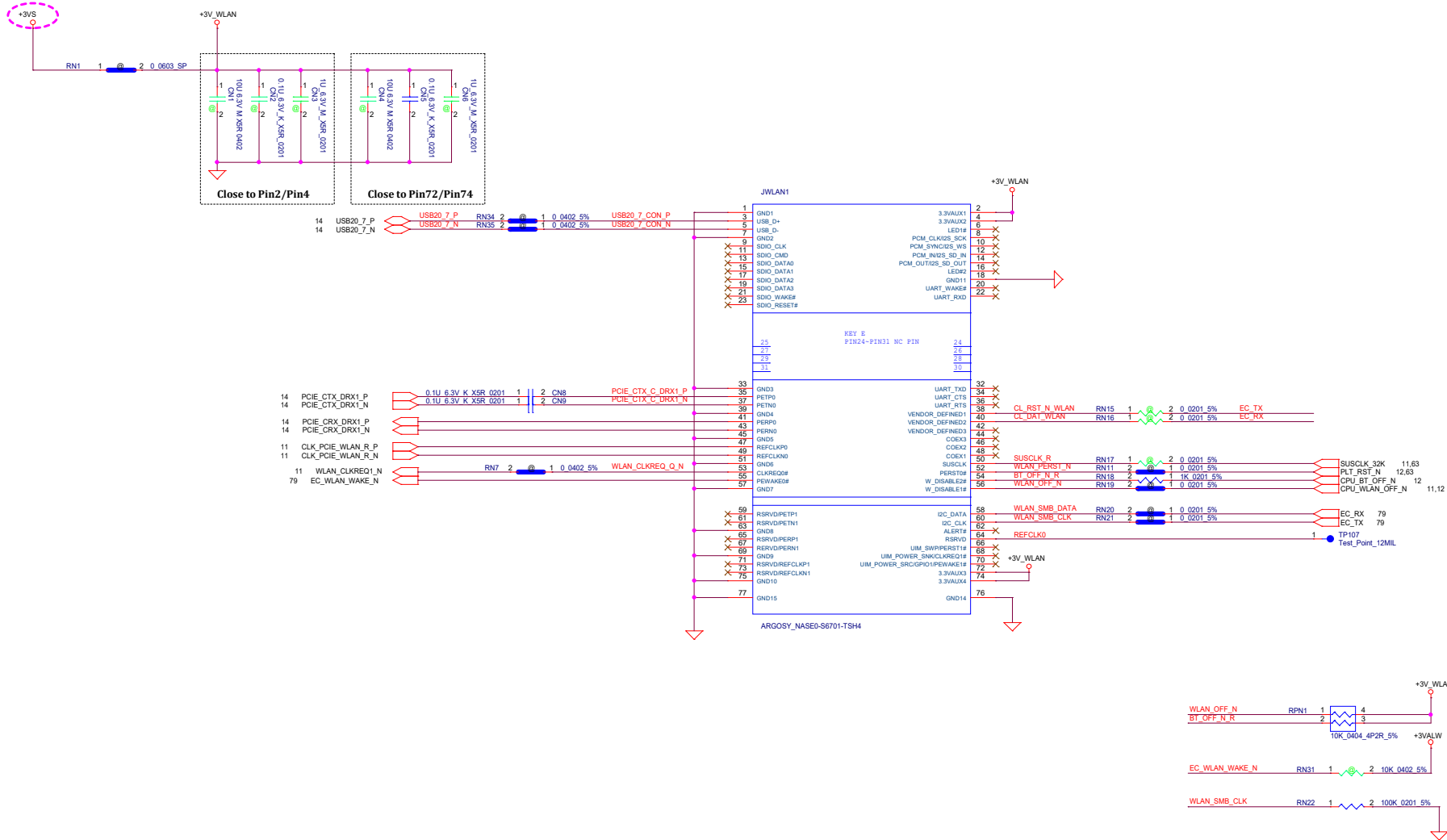


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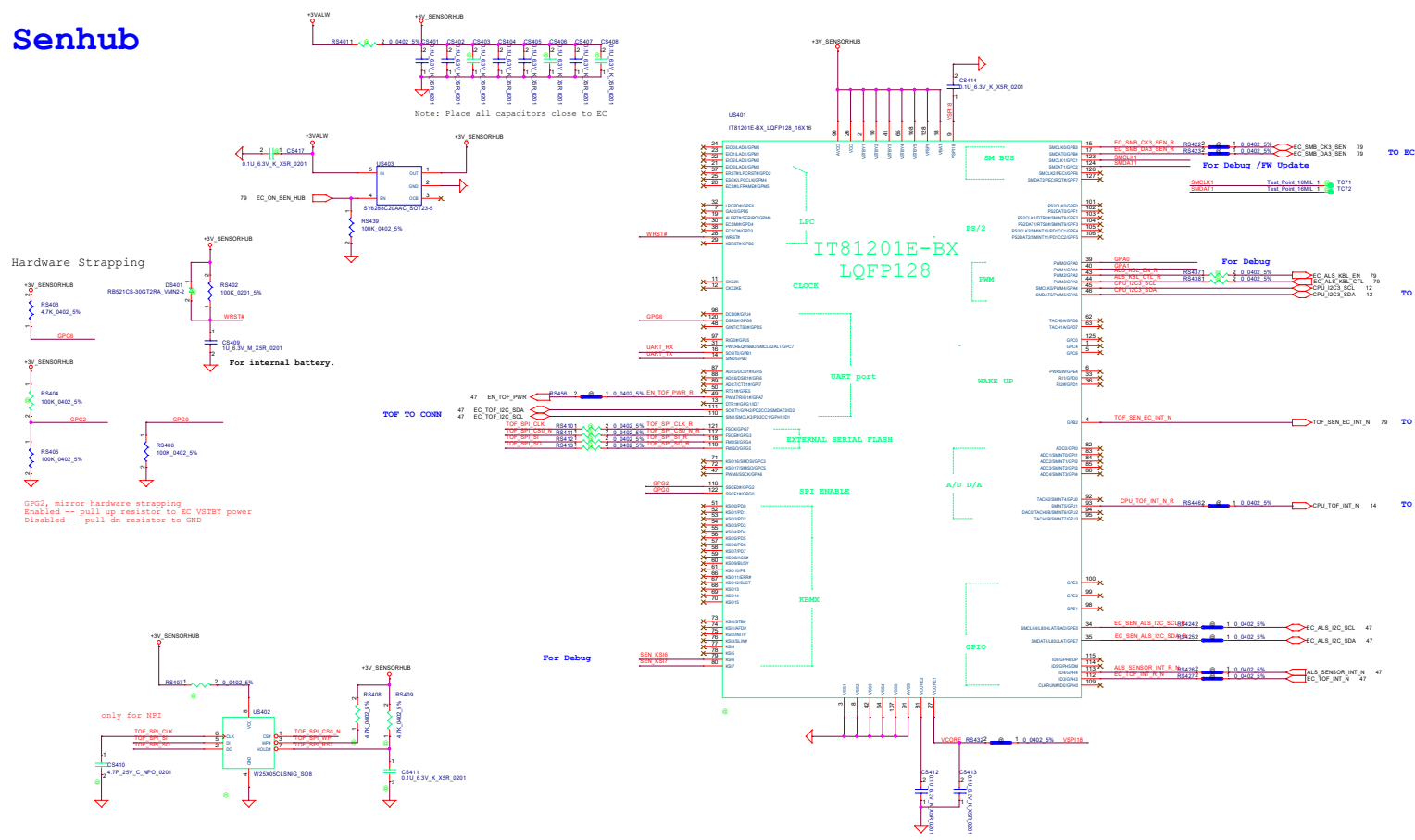
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<table><tr><td>Security Classification</td><td colspan="3">LCFC Highly Confidential Information</td><td>Title</td></tr><tr><td>Issued Date</td><td>2012/07/01</td><td>Deciphered Date</td><td>2014/07/01</td><td>S750-ARH</td></tr><tr><td colspan="4">THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.</td><td><table><tr><td>Size</td><td>Document Number</td><td>Rev</td></tr><tr><td>C</td><td>LAN CONN</td><td>0.1</td></tr><tr><td colspan="3">Date: Tuesday, January 05, 2021</td></tr></table></td></tr><tr><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td></tr></table>					Security Classification	LCFC Highly Confidential Information			Title	Issued Date	2012/07/01	Deciphered Date	2014/07/01	S750-ARH	THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				<table><tr><td>Size</td><td>Document Number</td><td>Rev</td></tr><tr><td>C</td><td>LAN CONN</td><td>0.1</td></tr><tr><td colspan="3">Date: Tuesday, January 05, 2021</td></tr></table>	Size	Document Number	Rev	C	LAN CONN	0.1	Date: Tuesday, January 05, 2021			5	4	3	2	1
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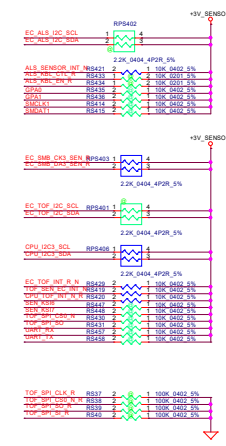


Notes

```
EC --> SMLCLK0/SMDAT0 [GPB3/GPB4] + interrupt [GPB2] (100/400KHz)
For Debug --> SMLCLK1/SMDAT1 [GPB3/GPB4]

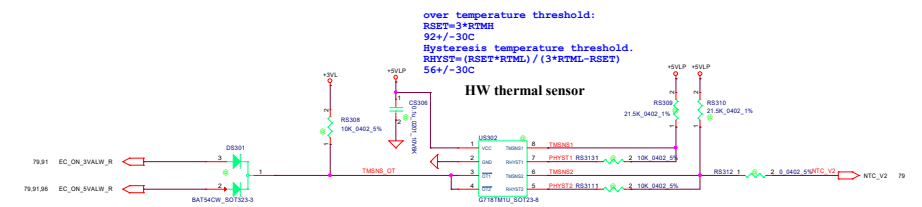
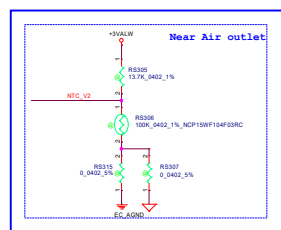
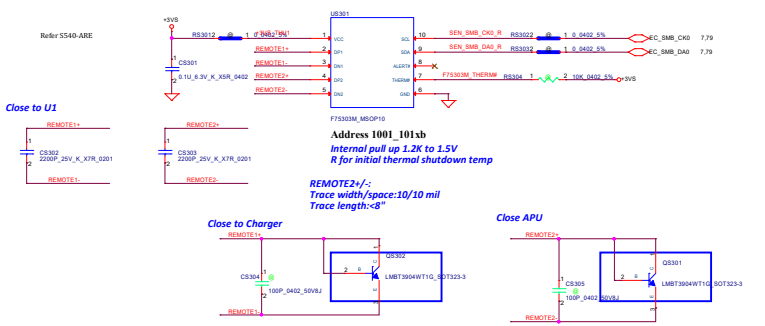
ToF -->SMLCLK3/SMDAT3[DMA] [GPH1/GPH2] + Interrupt [GPH3] _____
ALS/G -->SMLCLK4/SMDAT4[DMA] [GPG0/GPG7] (100/400KHz)
AMD --> SMLCLK5/SMDAT5[DMA] [GPA4/GPA5] + interrupt [GPJ1] 100/400KHz (By host control )
        [Preload code (HID Over I2C)]

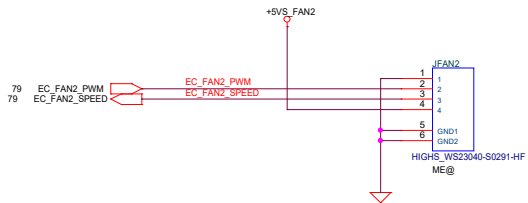
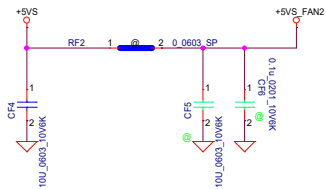
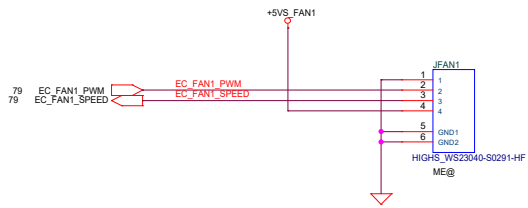
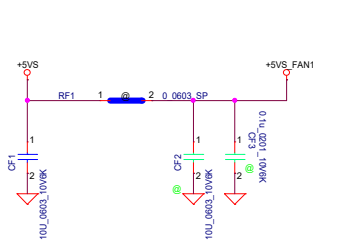
GPB0/GPB1/GPA0/GPA1 (GPIO x 4 (簡便))
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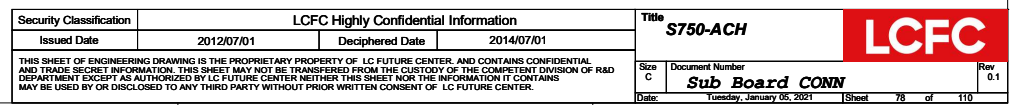


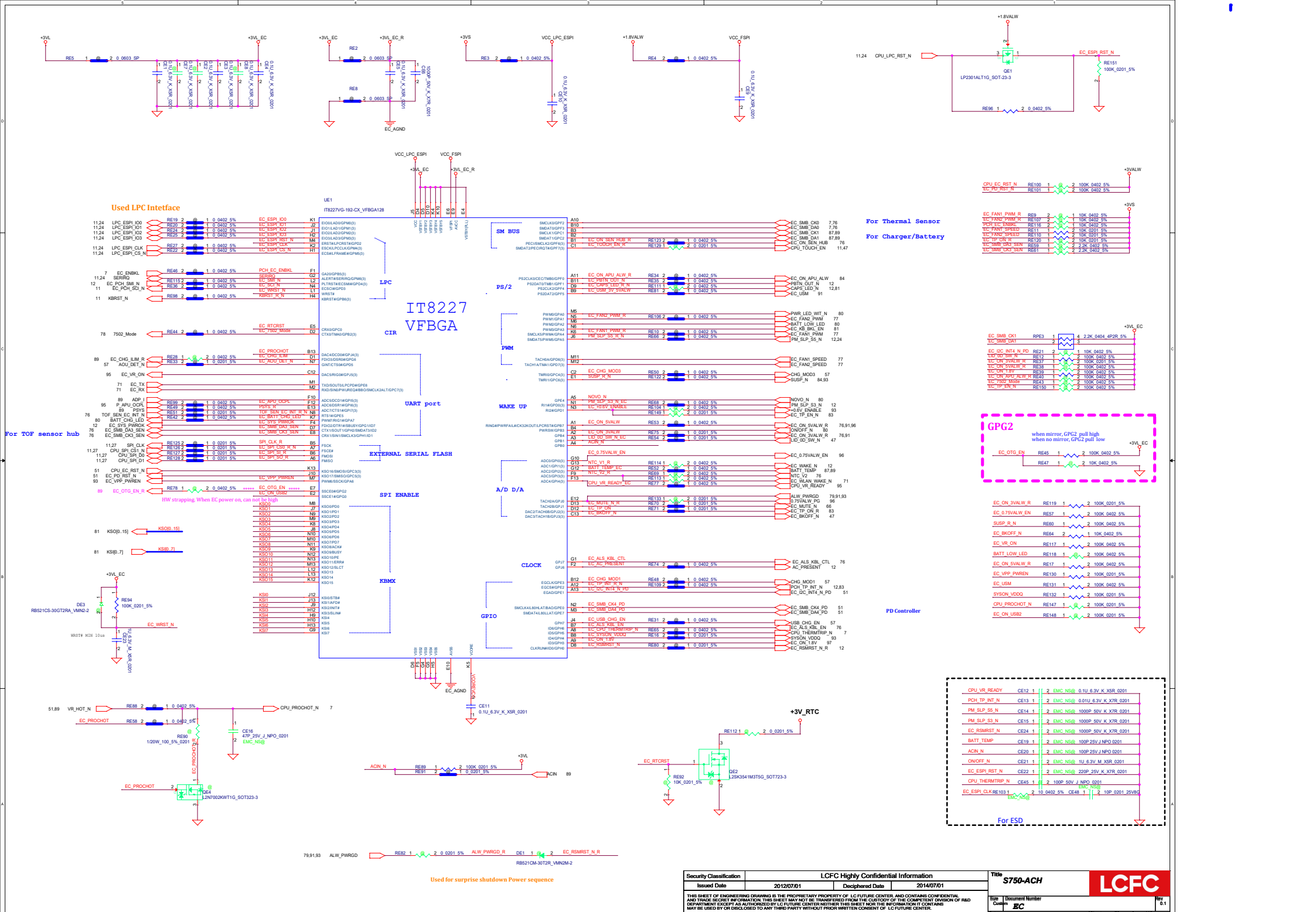
APU Thermal Sensor *Thermal Sensor
placed nearby SO-DIMM*

**Thermal Sensor
placed nearby SO-DIMM**

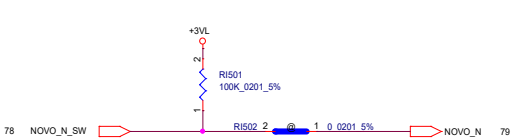
[illegible]



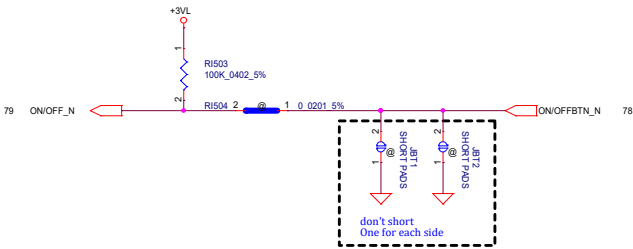




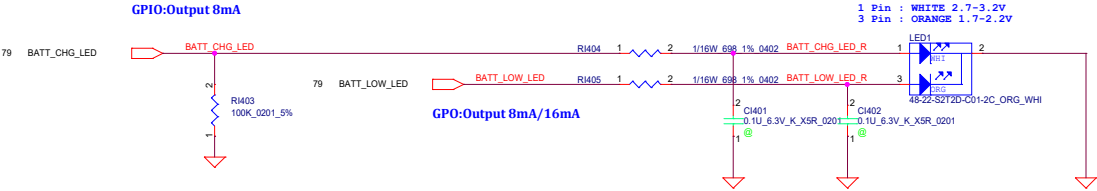
NOVO BUTTON



PWR BUTTON

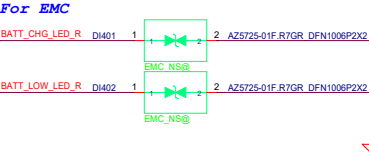
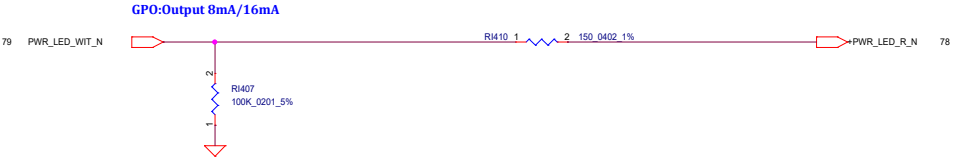


Charging LED



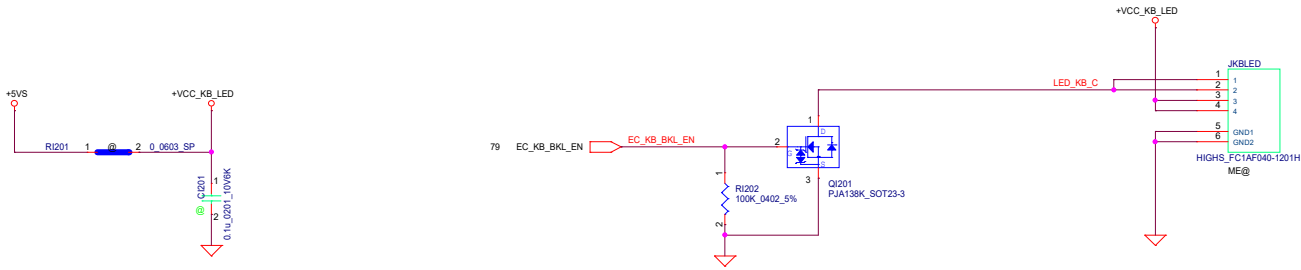
Power LED

Refer S540-ARE

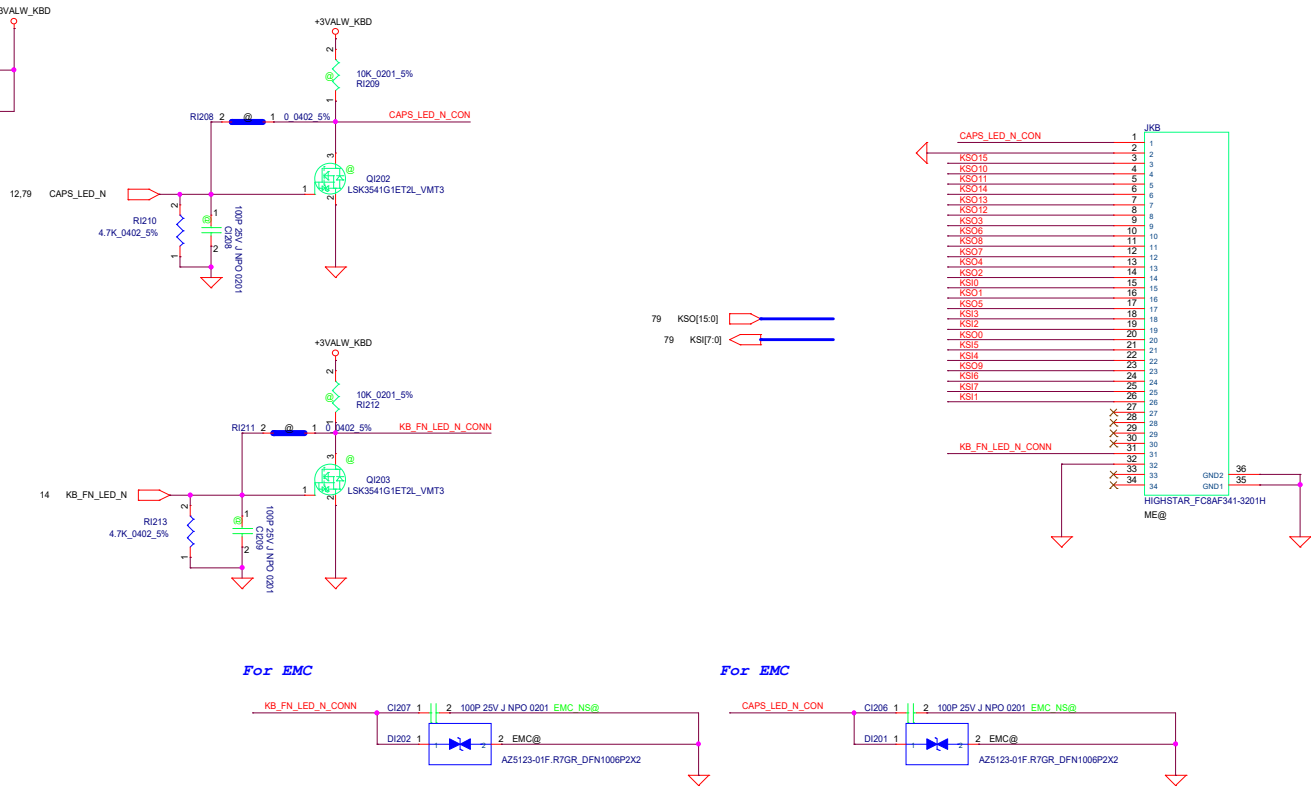


LED		State	LED Behavior
State (Same as the power button LED)	System on	White on (battery: 21%-100%)	Gradual is on , Gradual is off , 2s off
		500ms on, 500ms off (battery: 0%-20%)	
	Standby LED closed	System off	OFF
		Battery only	OFF
Charging	Charging	Amber on (battery: 1%-90%)	
		White on (battery: 91%-100%)	

KB Backlight Connector



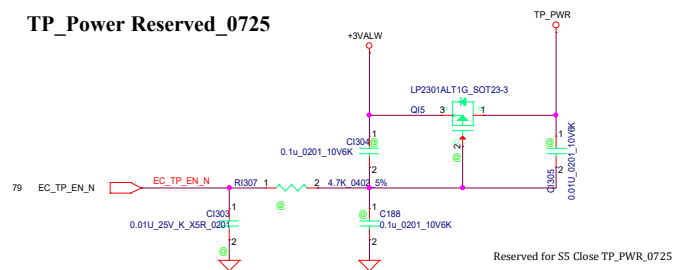
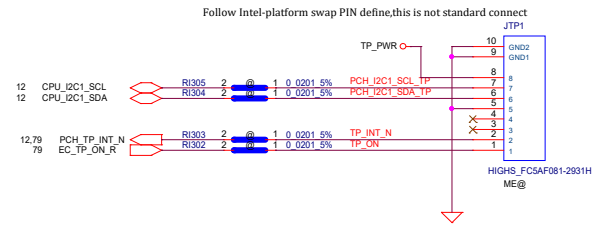
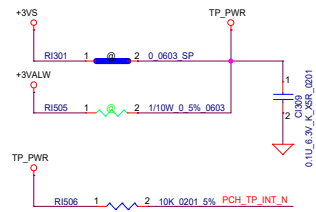
K/B Connector



5	4	3	2	1																																			
D				D																																			
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A				A																																			
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Issued Date	2012/07/01	Deciphered Date	2014/07/01	S750-ARH																																			
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				Date: Tuesday, January 05, 2021																																			
				Sheet 82 of 110																																			
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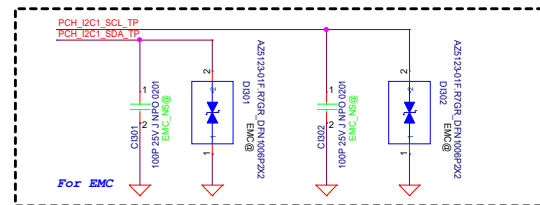
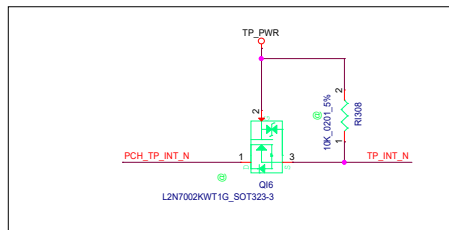
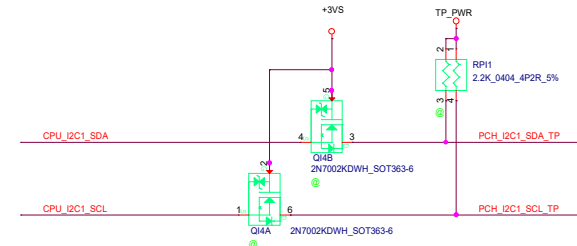
Normal TP



Reserved for S5 Close TP_PWR_0725

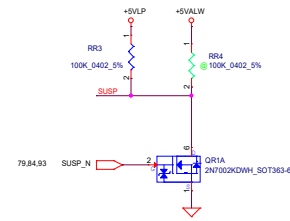
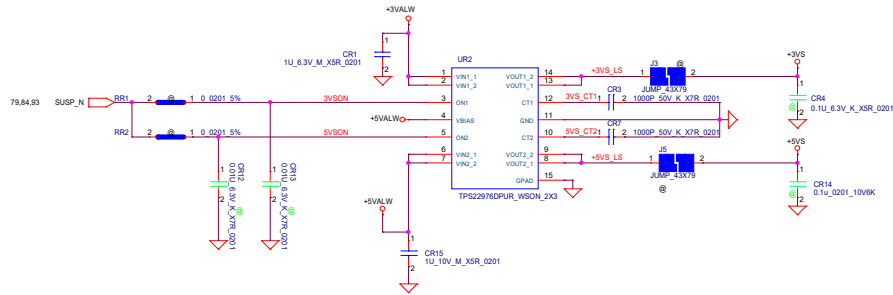


TP If use +3VALW power, need to levelshift_need to check_0702

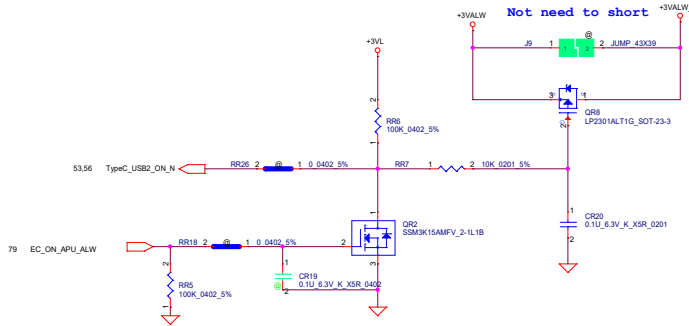


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Size		Document Number				Rev	
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Date:		Tuesday, January 05, 2021			Sheet	83	of 110

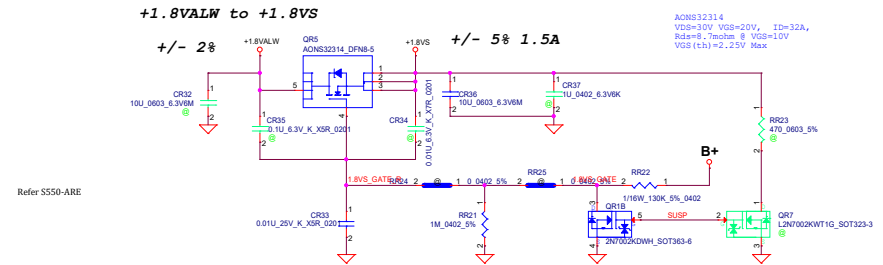
3VS/5VS



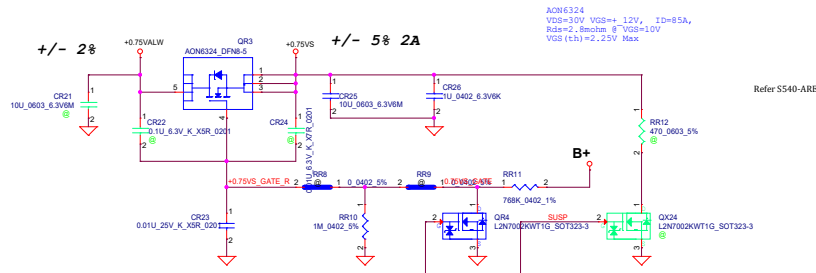
TO +3VALW_APU



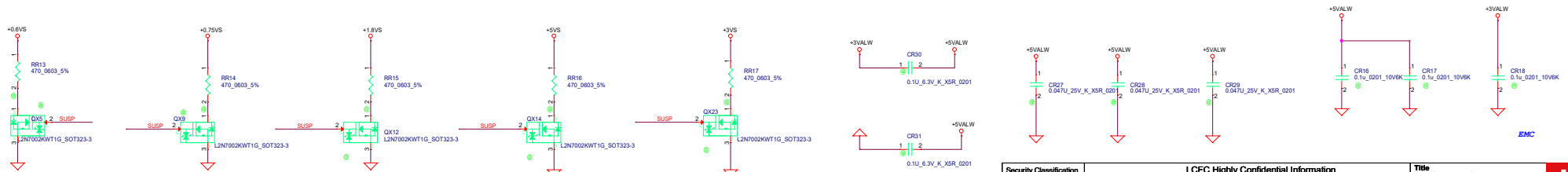
TO +1.8VS



TO +0.75VS



For DisCharge



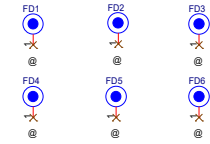
A		B		C		D		E	
1									
2									
3									
4									
				</					

CPU

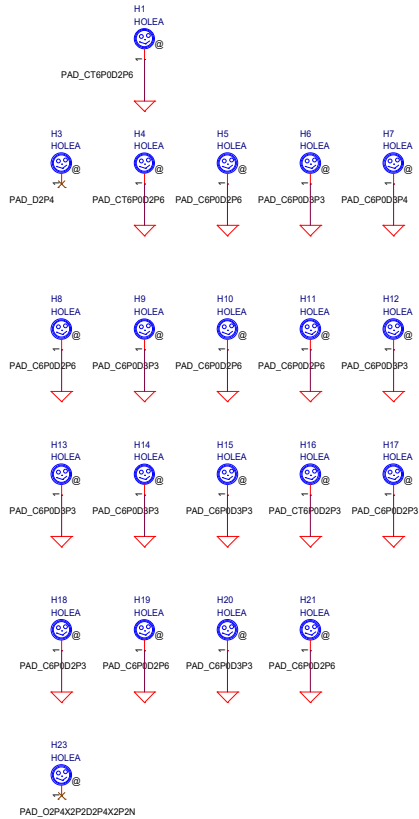
GPU

Memory Shielding

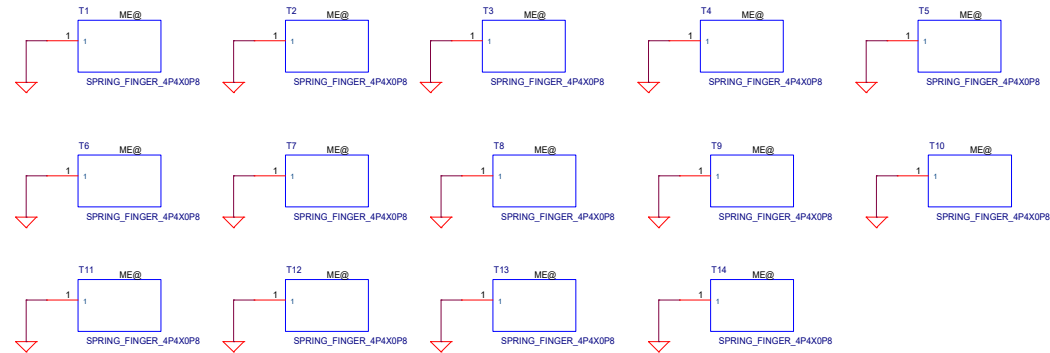
PCB Federal Mark PAD

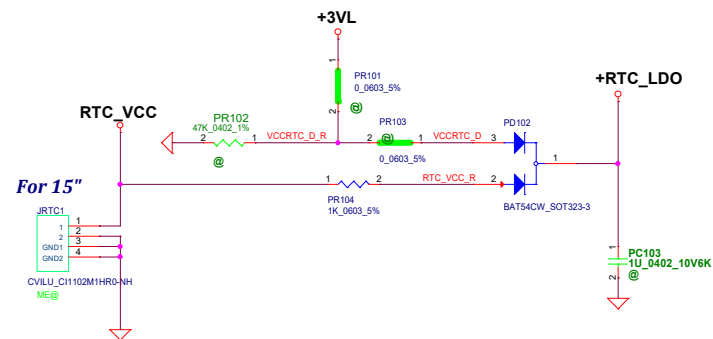


Hole

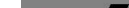





Shielding

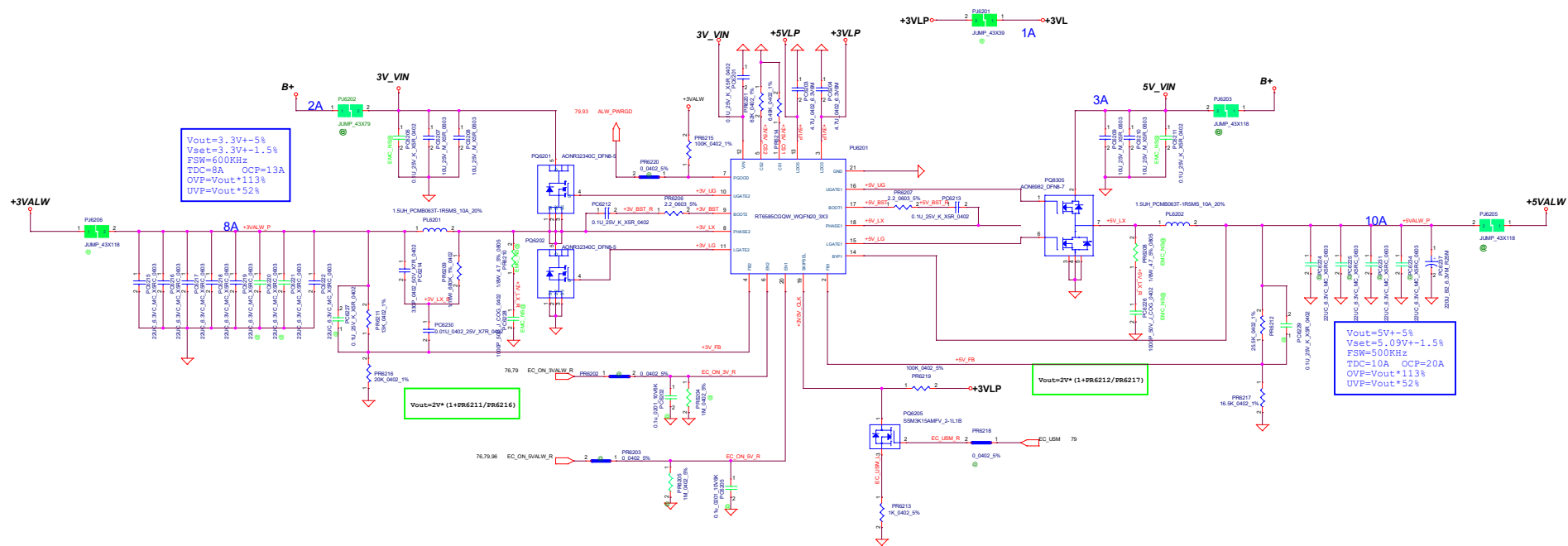




For 15"

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Issued Date	2018/08/02	Deciphered Date	2018/08/02	PWR_DCIN/RTC	
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Size	Document Number	Y560 AMD			Rev
C					0
Date:	Tuesday, January 05, 2021	Sheet	87	of	110

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A				A																																
<table><tr><td colspan="2">Security Classification</td><td colspan="2">LC Future Center Secret Data</td><td colspan="2">Title</td><td rowspan="2"></td></tr><tr><td>Issued Date</td><td>2018/08/02</td><td>Deciphered Date</td><td>2018/08/02</td><td colspan="2">PWR_Memory PWR Decoupling</td></tr><tr><td colspan="5" rowspan="2">THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.</td><td>Size</td><td>Document Number</td><td>Rev</td></tr><tr><td>B</td><td>Y560 AMD</td><td>0.1</td></tr><tr><td colspan="5"></td><td>Date:</td><td>Tuesday, January 05, 2021</td><td>Sheet 90 of 110</td></tr></table>					Security Classification		LC Future Center Secret Data		Title			Issued Date	2018/08/02	Deciphered Date	2018/08/02	PWR_Memory PWR Decoupling		THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.					Size	Document Number	Rev	B	Y560 AMD	0.1						Date:	Tuesday, January 05, 2021	Sheet 90 of 110
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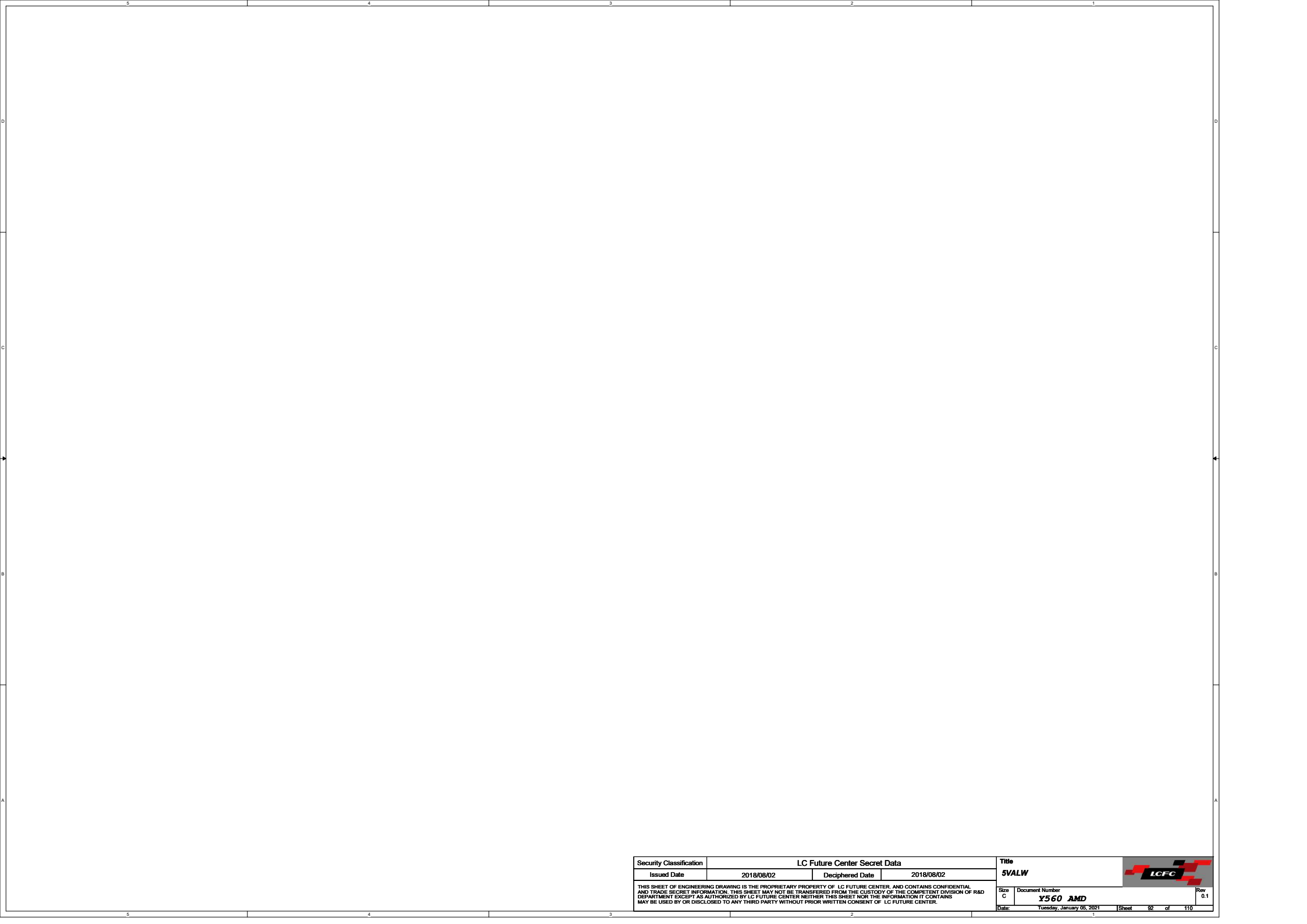
	RT6585C	RT6575D&TPS51275B
Mode	DEM/USM	USM/CCM
3V FSW	600K	355K
5V FSW	500K	300K
CSx	$X_{limit} = (I_{limit} \times R_{daon}) \times 8 / 50uA$	$X_{limit} = (I_{limit} \times R_{daon}) \times 8 / 10uA$


RT6585B&TPS51285B BOM to BOM

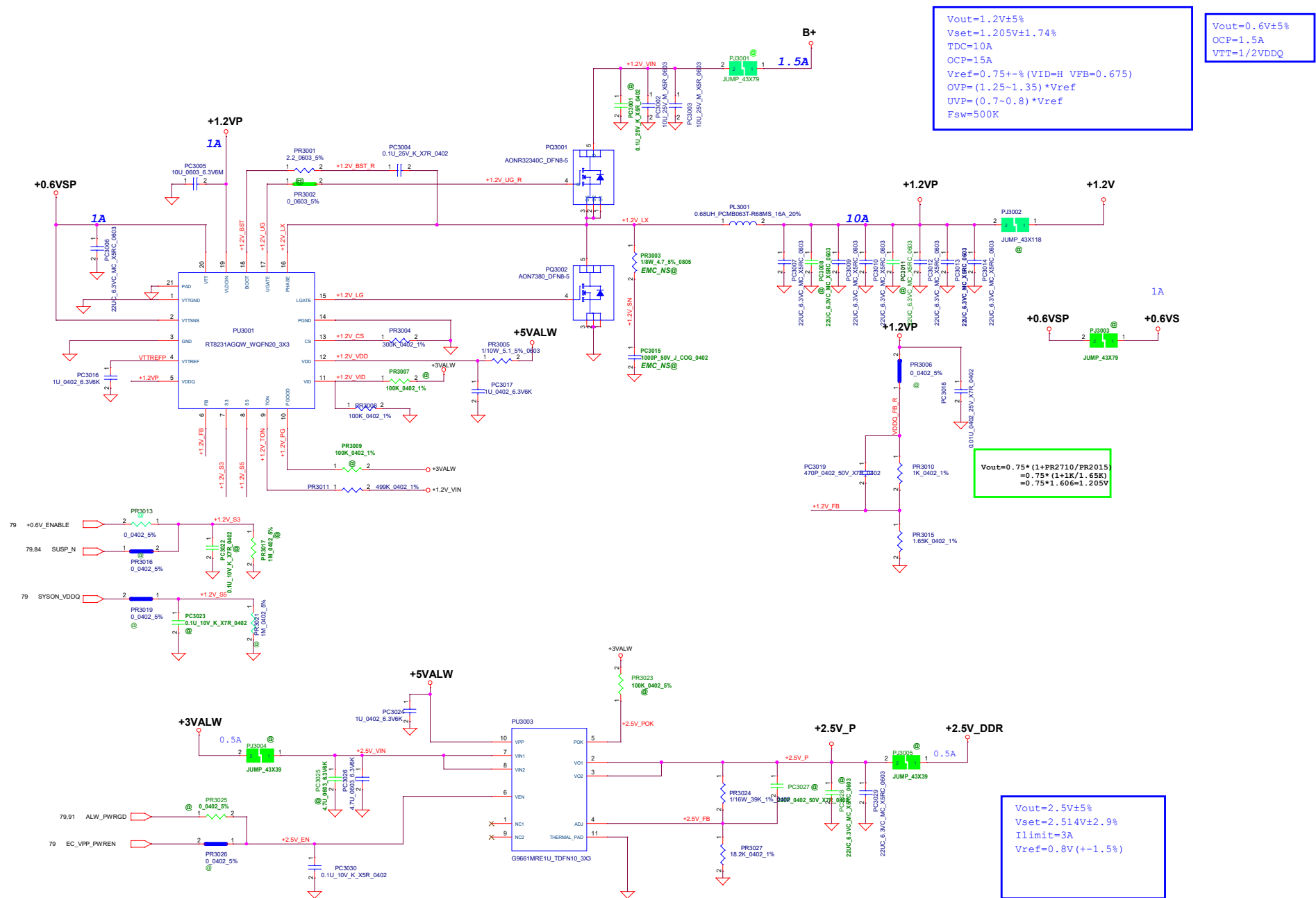
RT6575D&TPS51275B BOM to BOM

RT6585B&RT6575D PIN to PIN, with different work mode, FSW, and CS setting

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Issued Date	20160701	Design Date	20140701	
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Rev	1	Drawn	PWR 3VALN/5VALN	01
Date	2016.07.01	Issued	01	of 110



Security Classification		LC Future Center Secret Data		Title			
Issued Date		2018/08/02	Deciphered Date	2018/08/02	5VALW		
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Size	Document Number			Rev			
C	Y560 AMD			0.1			
Date: Tuesday, January 05, 2021				Sheet		82	of 110



STATE	EN1	EN2	VDDQ	VTT_REFP	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

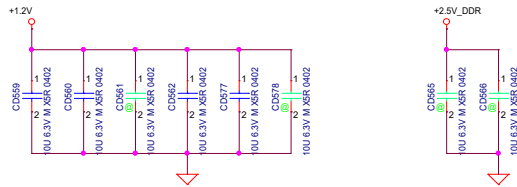
Note: S3 - sleep ; S5 - power off

Address	0X6A	0X68	0X66	0X64	0X62	0X60
TOP R (Kohm)	OPEN	3.9	3	2.3	1.3	10
BOT R (Kohm)	10	1.3	2.3	3	3.9	OPEN
Bus_sel Volt (% of VCC)	0%	25%	40%	60%	75%	100%

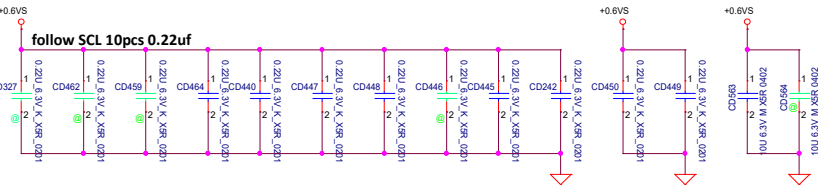
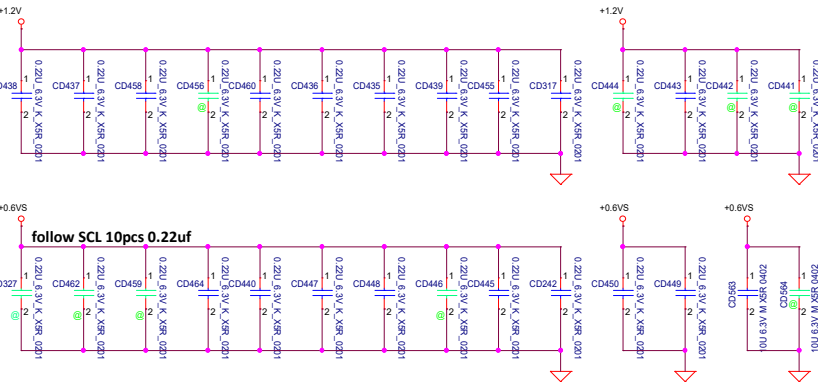
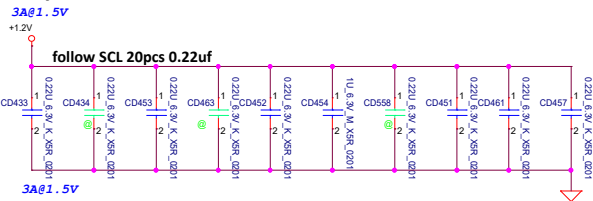
Table 32. DDR4 DRAM Down Per-Channel Decoupling Capacitors

Capacitor		Configuration	VDDIO_MEM_S3-VSS	VDDIO_MEM_S3-VTT	VTT-VSS	VREF_CA- VDDIO_MEM_S3
Value	Package Size / Material					
0.1 μ F	0402 X5R	SRx16	-	-	-	4
0.22 μ F	0402 X5R	SRx16	18	5	5	-

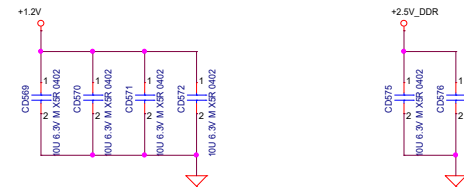
EE side Channel A



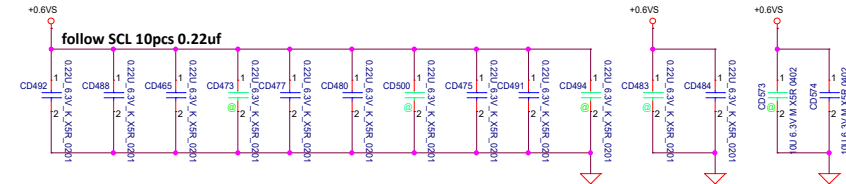
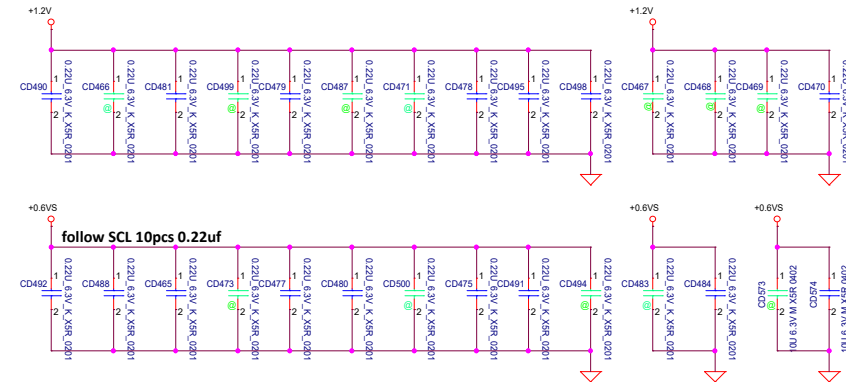
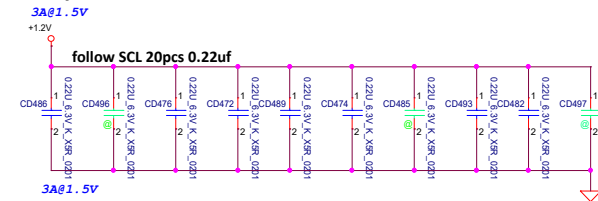
Layout Note: Place near DRAM



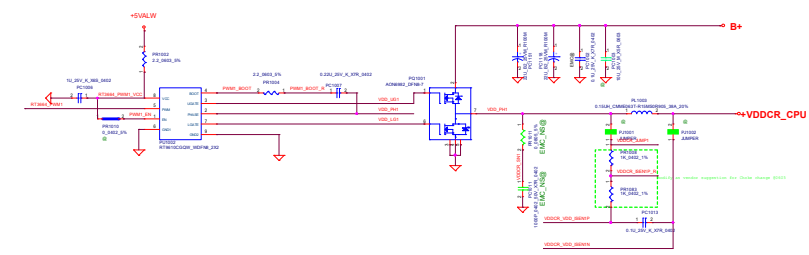
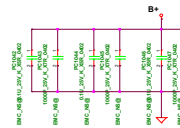
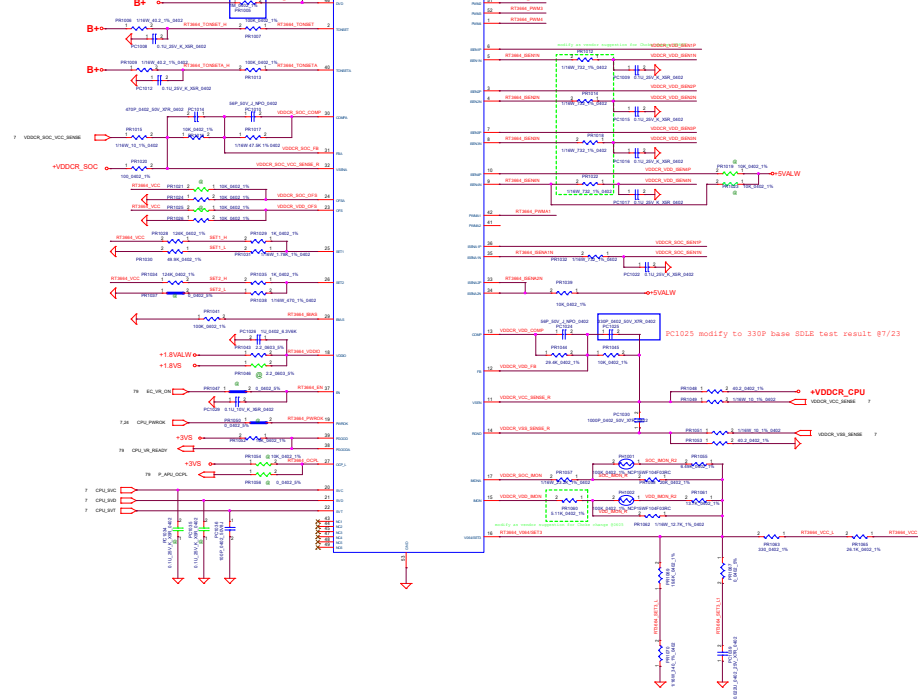
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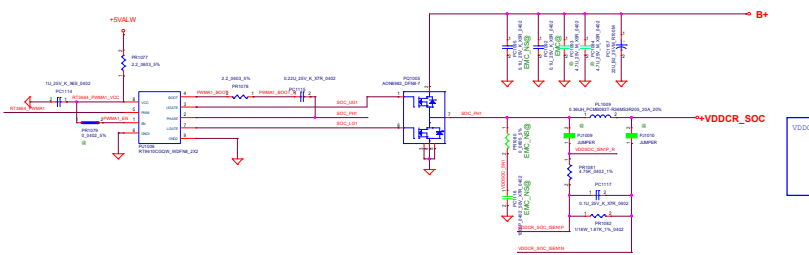
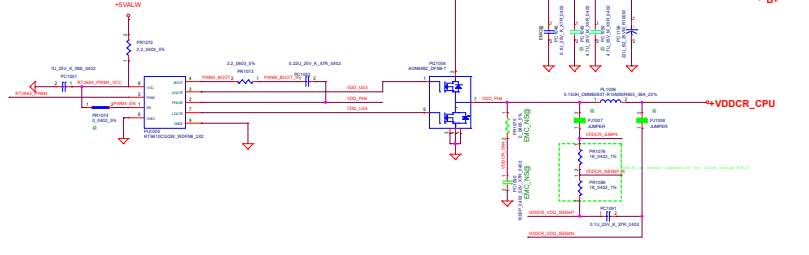
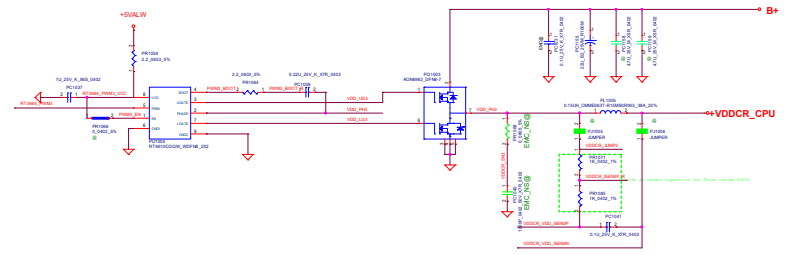
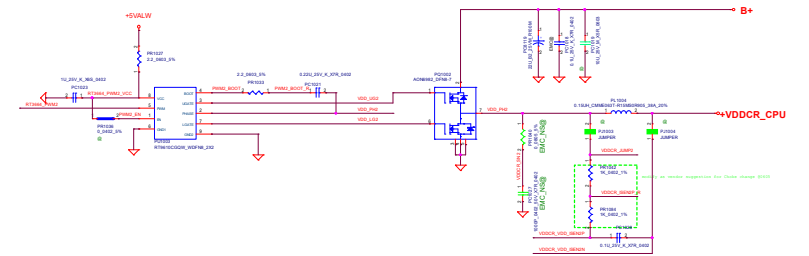
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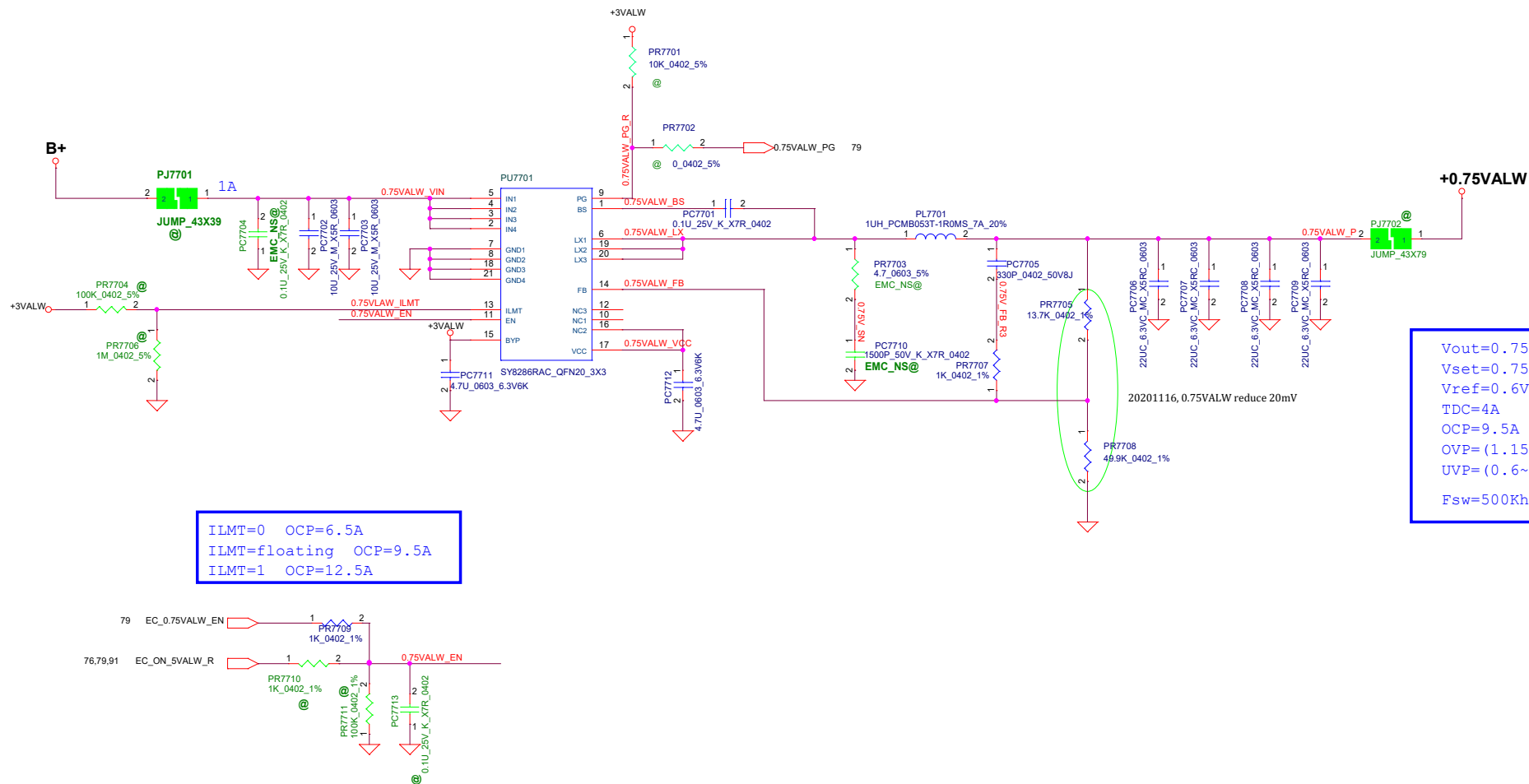
PR5109 1M FOR 48 battery,
39 battery need change to 787K




FOR Cezanne 418
VDDCR_VDD1TDC=98A PR=110A



VDDCR_SOC1TDC=15A PR=20A

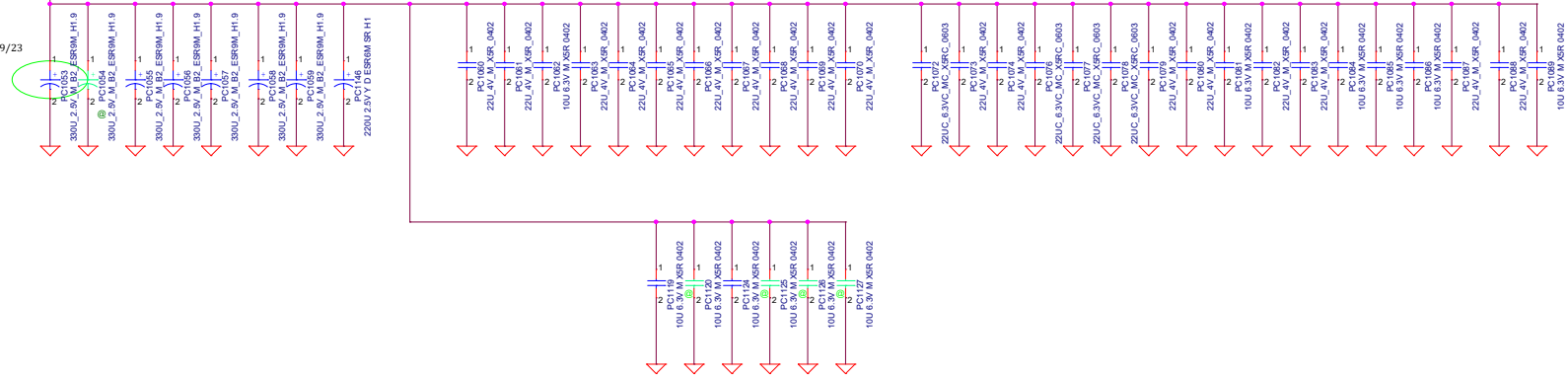


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stuff for Cezanne platform 09/23

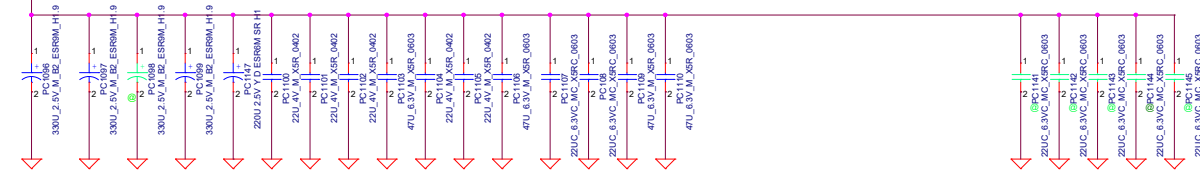
+VDDCR_CPU


Vendor suggest: 330uF*7PCS+22uF*30PCS
actual test: 330uF*5pcs+22uf*15pcs+10uf*15pcs

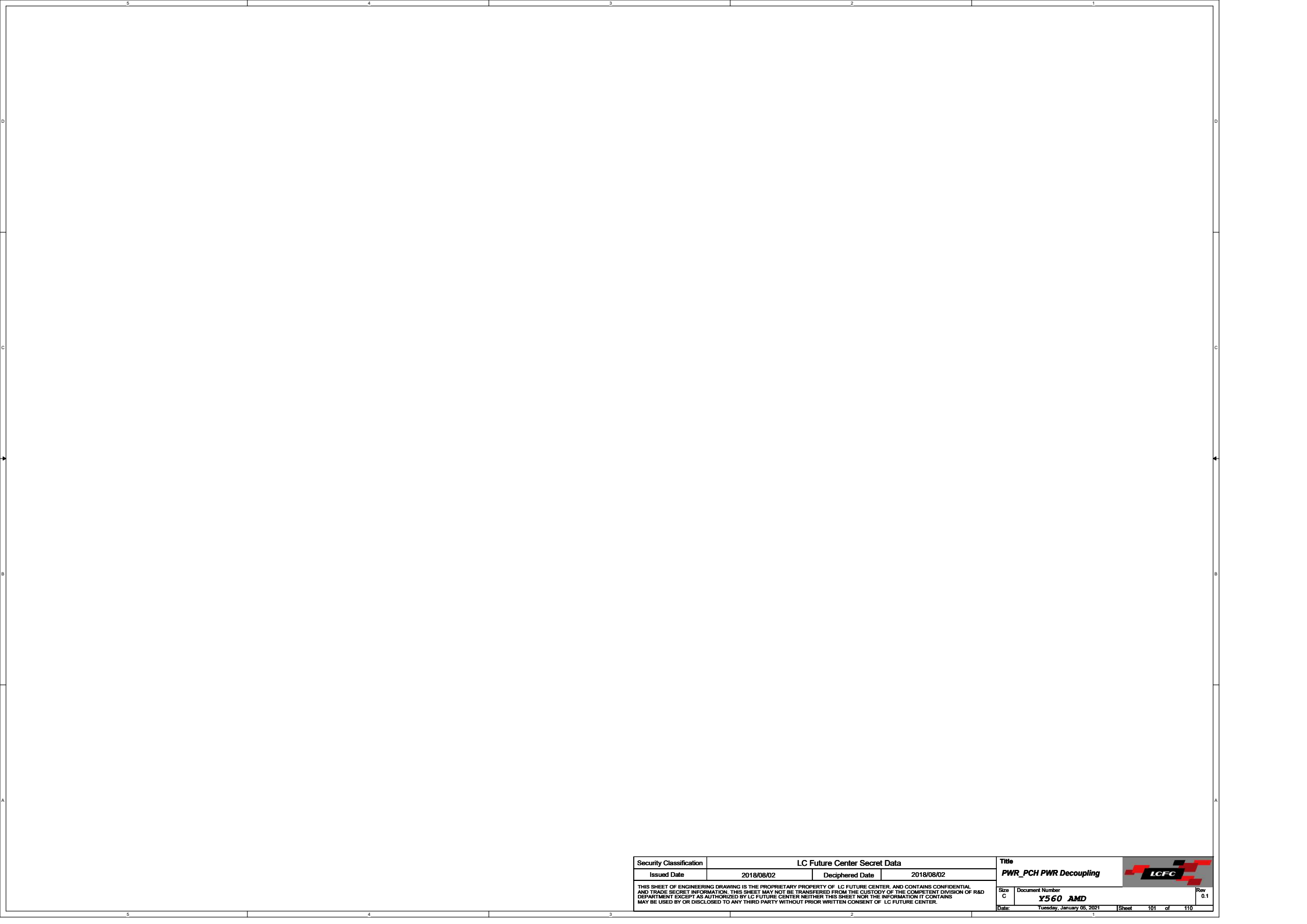



+VDDCR_SOC


Vendor suggest: 330uF*1PCS+470uF*1pcs+22uF*12PCS
actual test: 330uF*3pcs+10uf*8pcs+22uf*7pcs




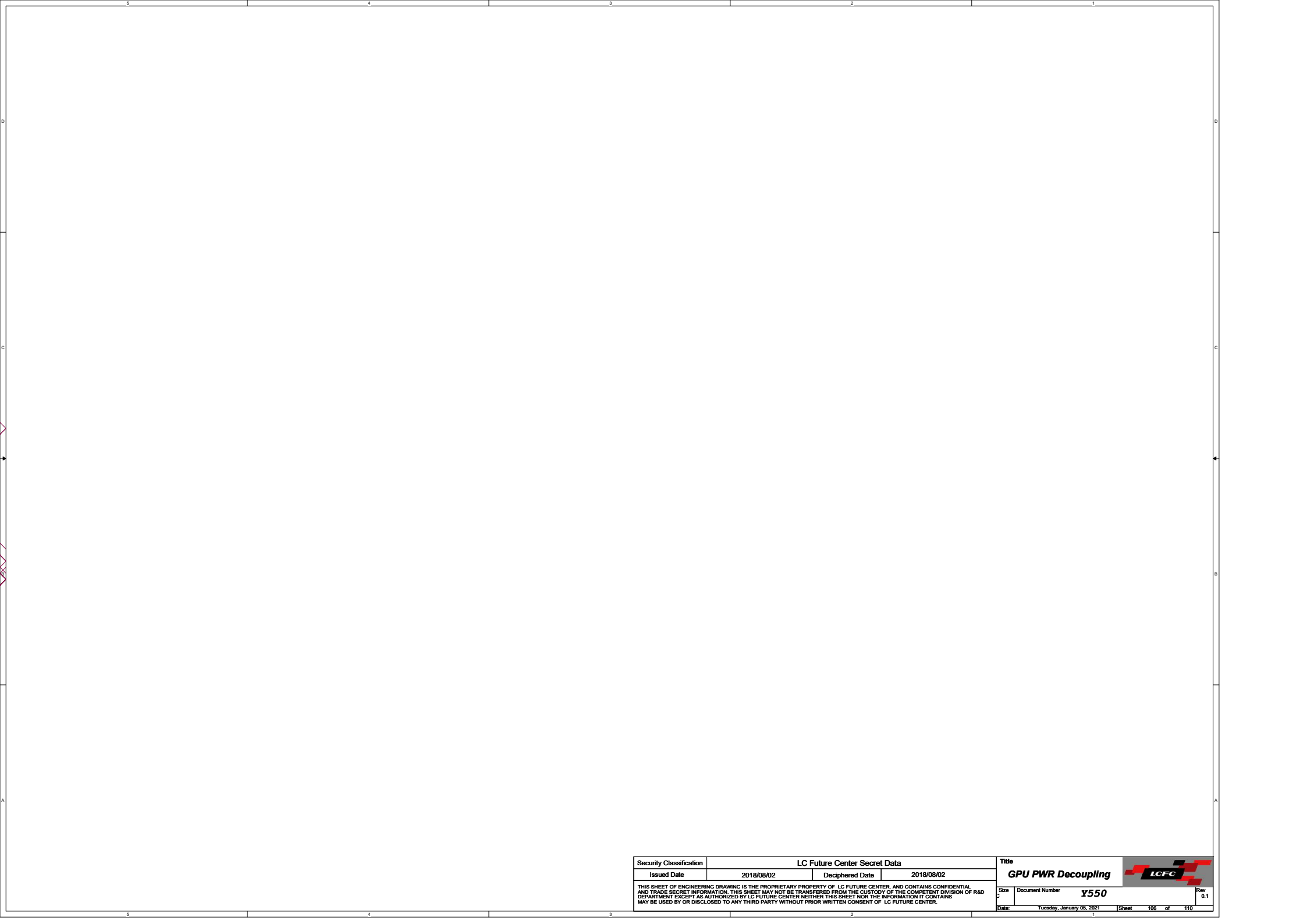
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D				D															
C				C															
B				B															
A				A															
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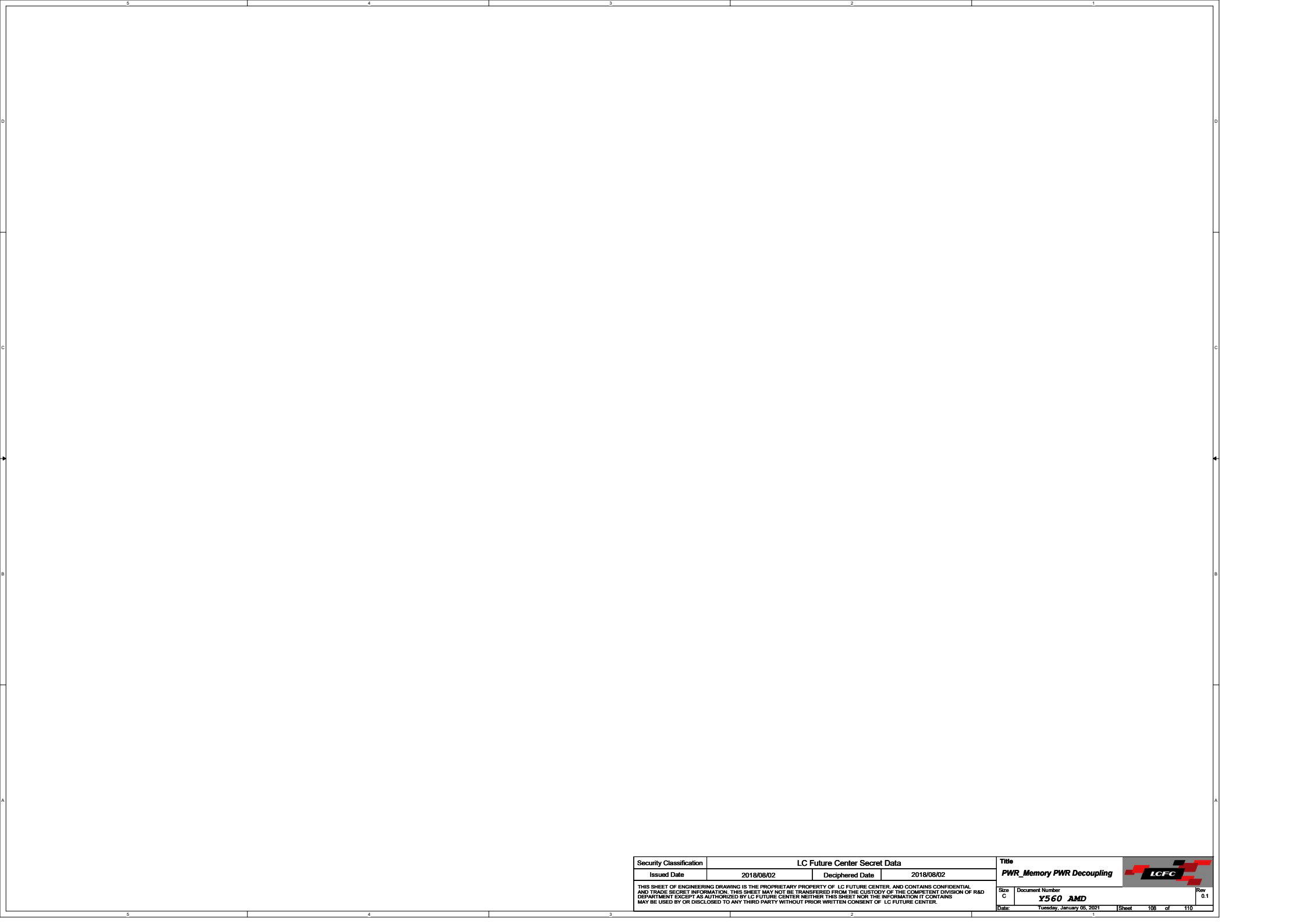
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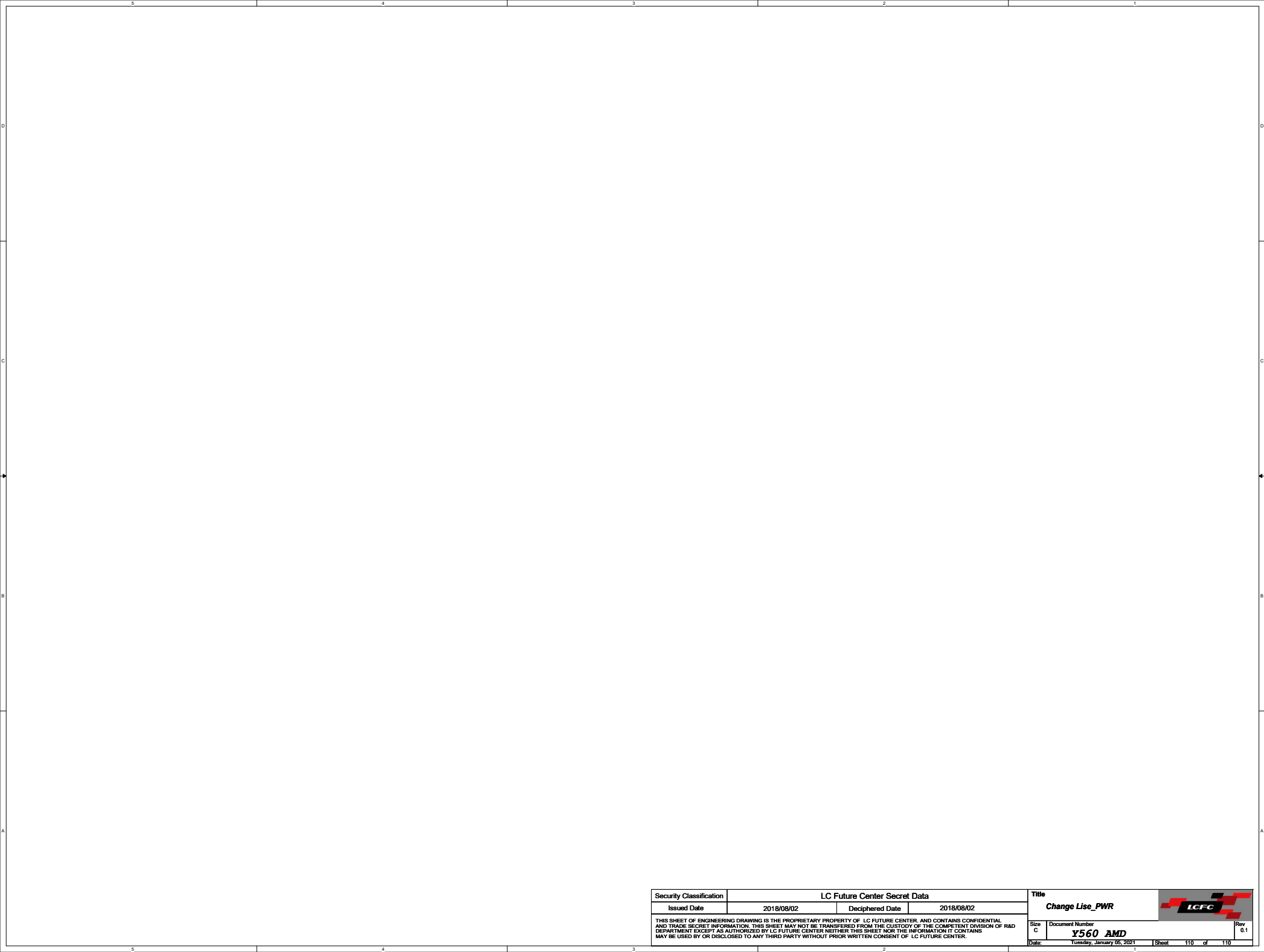
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